Send High-Speed ADC Data Remotely And Quietly

Application Brief 124

Robert LeBoeuf

Highlights

- **Integrated LVDS Output Drivers Onboard the ADC**
- **Minimal Number of Wires Required at the ADC Output**
- **Differential Signaling for Minimal Common Mode Interference**
- **Smaller Number of Data Lines Saves PCB Space**

In the world of Analog-to-Digital conversion, it is often desired to transport the digital data downstream using a minimal group of wires. This problem is sometimes addressed by using ADCs that are serial data output capable. This solution however, has its set of challenges. Serial output ADCs are often lower speed due to the limitations inherent with traditional serial busses. Such busses often use single-ended signaling, which can become a source of EMI for surrounding circuitry. They can also be subjected to common-mode noise from surrounding circuitry, which can induce errors in the data transmission.

One way of overcoming some of these problems is to use an LVDS (Low Voltage Differential Signal) data bus. *Figure 1* shows a block diagram of an ADC with an LVDS output, driving an ASIC or a deserializer:

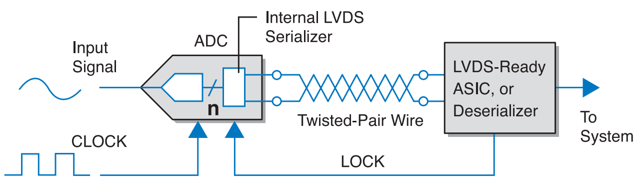

Figure 1: Block Diagram

Here the ADC outputs a serial data stream using the LVDS signal format. At the receiver end, an LVDS-ready ASIC, or a deserializer recovers the n-Bit output.

During the power-up sequence, the ADC and the receiver go through a two-step initialization sequence. This initialization refers to the synchronization of the PLLs that would be contained in each chip. First, the receiver locks to a frequency provided by an oscillator. The ADC PLL locks to CLKIN. After this, the ADC sends out a data sequence referred to as a 'SYNC' pattern. This is a pattern of any number of ones followed by the same number of zeros, clocked at the output data rate. The PLL inside the receiver locks to this SYNC pattern, and sends a 'LOCK' signal back to the ADC. This signals the ADC that the receiver is locked, and is ready for incoming data. The output data is composed of a 'start-bit' which is always a '1', n bits of data, and a 'stop-bit' which is always a '0'. *Figure 2* shows a flow chart that summarizes this sequence:

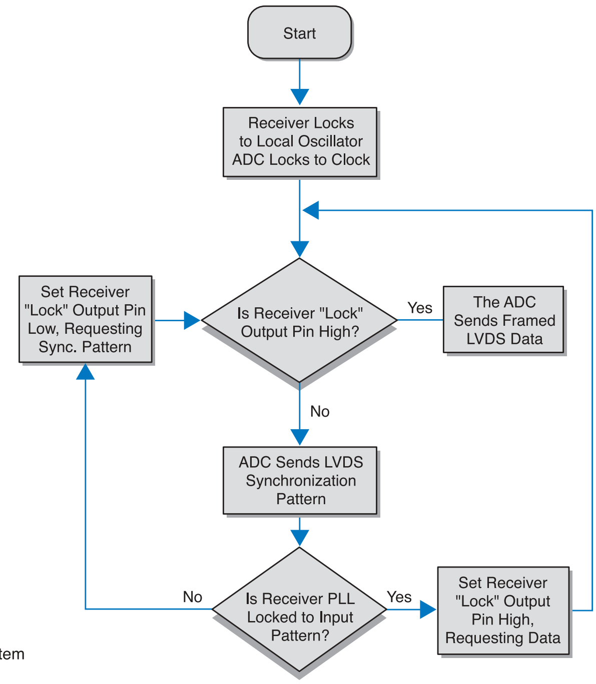

Figure 2: Flow Chart

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This FRAME is therefore made up of n+2 bits. The datastream frequency is therefore (n+2) x f_{sample}. The receiver may keep receiving data as long as its PLL remains locked. If it slips out of lock, the LOCK line is set low, and the ADC is asked for the synchronization pattern again.

The output drivers of the ADC are current sources capable of driving a 100Ω twisted-pair line, a PCB slot line or microstrip line. *Figure 3* shows two typical termination schemes that are used near the receiver:

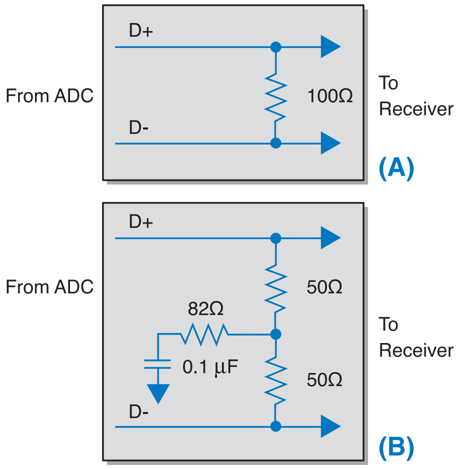

Figure 3: Typical Termination Scheme

Figure 3A shows a simple termination scheme. The resistor terminates the line from the ADC reducing any reflections that may occur. It also provides a load that the current sources need to produce the output signal. *Figure 3B* also shows a simple termination scheme, but offers a common mode resistance to dampen the cable if needed. This method is a little less common. In addition to a minimal number of wires between the ADC and the deserializer, the differential signal format keeps the magnetic fields tightly contained around the transmission line. This reduces the EMI of these wires, which may cause problems in nearby circuitry.

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National Semiconductor
2900 Semiconductor Dr.
PO Box 58090
Santa Clara, CA 95052
1-800-272-9959

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