

# LMH0340 / LMH0341 SerDes Family LVDS Timing Overview

National Semiconductor  
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## Introduction

The LMH0340 and LMH0341 were designed to allow low cost FPGAs to be used in the implementation of advanced Serial Digital Interfaces, up to and including the 3 Gbps interface. They feature advanced on-chip signal and clock conditioning circuitry that extends data transmission reach with Belden 1694A or comparable broadcast video cable over 300m (for Standard Definition Video) with the use of an external cable equalizer such as the LMH0384.

The SerDes unique architecture is designed specifically to address the interface requirements of low cost FPGA devices. The 5-bit LVDS parallel data interface simplifies board layout by reducing the number of input/output (I/O) pins and traces between the serializer, deserializer and the FPGA. The 5 bit wide interface was chosen so that the data rate of the 3 Gbps signals would be brought down under 600Mbps where it can be handled by the I/O of low cost FPGA devices. This application note explains the LVDS timing requirements for the LMH0340 and LMH0341 family of products.

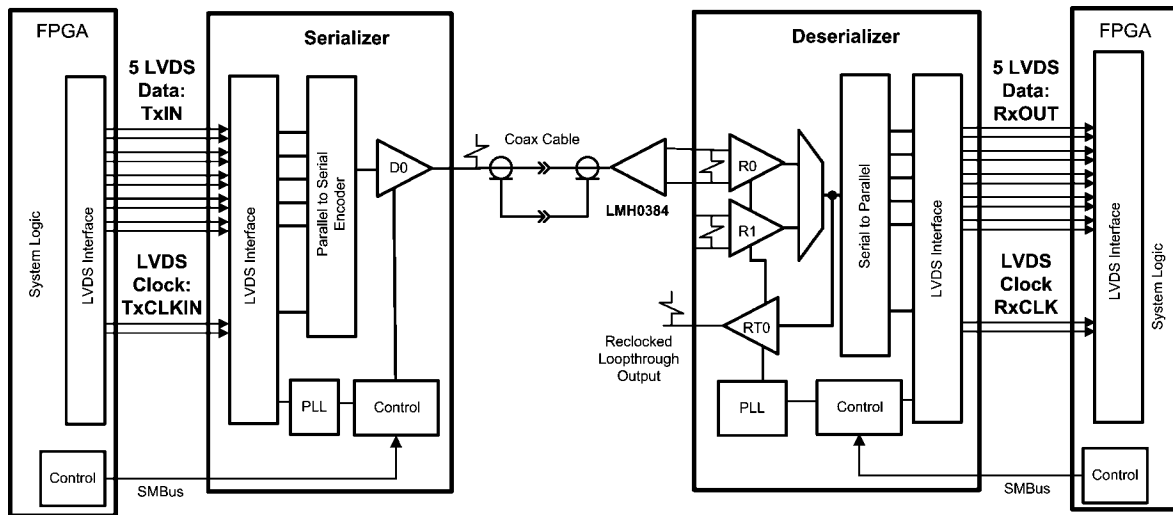
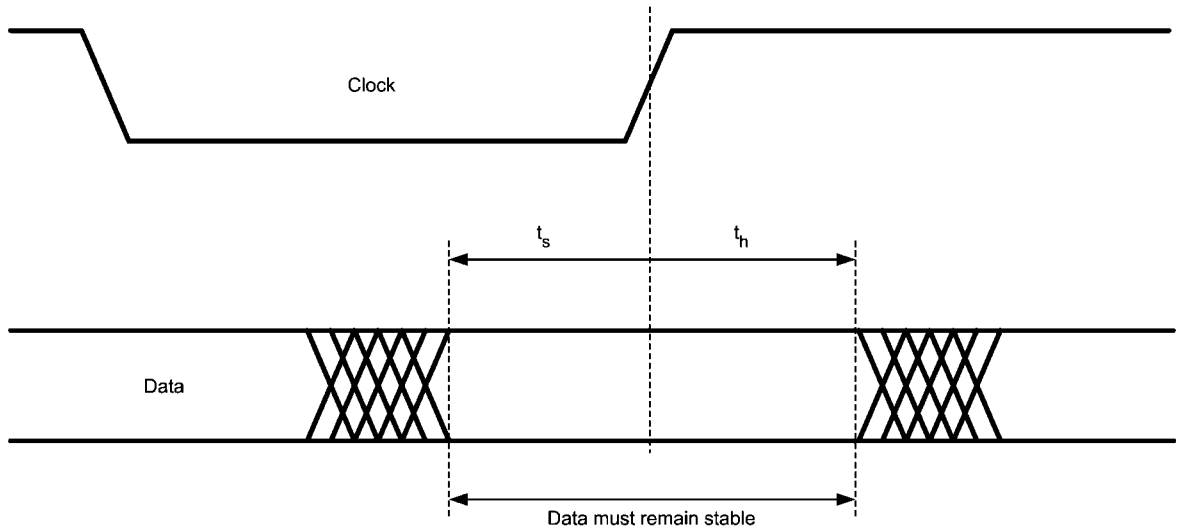


FIGURE 1. FPGA-Attach System Diagram

## Serializer Device Timing Requirements

Consider how a simple register such as the 74LS174 D Flip Flop is specified, there is a single clock edge sampling a single data edge. The clock samples the data on a single edge, either positive or negative depending on the flip-flop. The set-

up time is on the order of 10's of nanoseconds and hold times very close to 0. The optimal clock position for the flip-flop is in the middle of the bit period of the data, as seen in the diagram below, although with a 0 hold time, it is also possible to implement systems in which the clock and the data all switch at the same time.

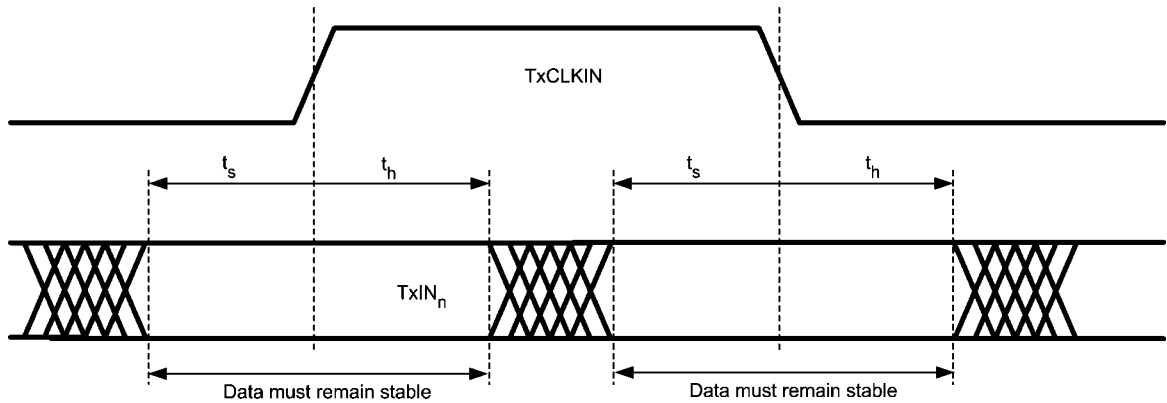


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**FIGURE 2. Single Clock Sampling Data Setup and Hold Time**

For Dual Data Rate (DDR) interfaces, the clock samples the data on both edges of the clock. CMOS, LVPECL or LVDS interfaces can utilize a DDR interface. The main advantage of DDR interfaces is the clock and data frequency are identical which maximizes data throughput for the protocol. The duty cycle distortion of the clock plays a critical part in the setup and hold time as both edges must meet the setup and hold time requirements to sample the data in the mid-bit transition.

Note that if there is skew between the various data lines, or if there is duty cycle distortion of the clock, all of these non-idealities work to reduce the amount of timing margin in the system, so all effort should be taken to reduce inter-pair data skew and clock distortion.



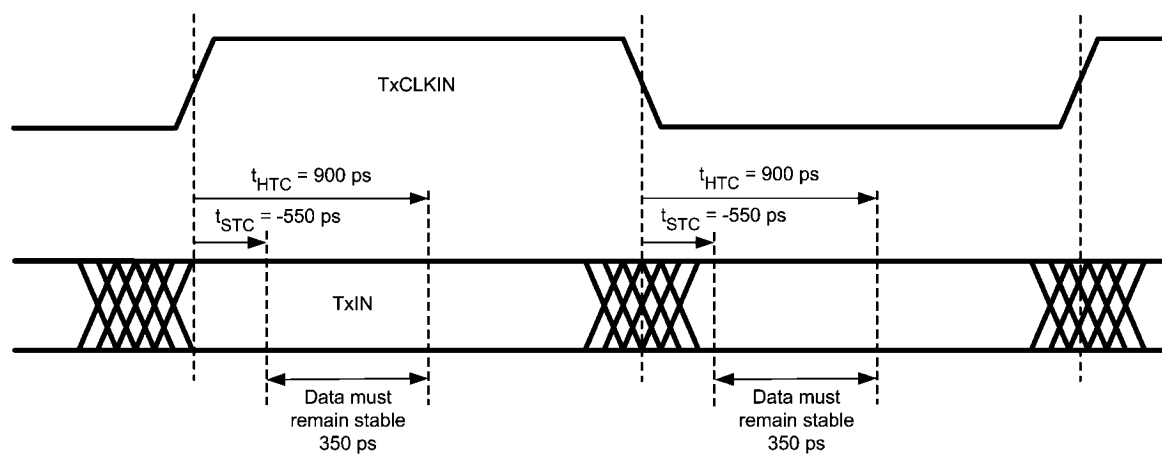
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**FIGURE 3. DDR Interface Setup and Hold Time**

The LVDS DDR input implementation in the Serializer reduces the number of Clock / PLL resources required in the host FPGA. The setup and hold time requirements for the LVDS Interface input latch expects the alignment of the clock and data transitions. An additional clock resource is not needed to offset the clock edges in the middle of the data bits.

The numbers that are specified in the datasheet (minimum setup time is -550 ps and the maximum hold time is 900 ps) are worst case numbers and by assuring that each of your data lines meets these timing requirements, you are guaran-

teeing that the device will properly latch it's input data. A negative setup time comes about because within the device there is a delay on the clock line that allows the FPGA to shift out the clock and data on the same clock edge. Internal to the Serializer, the clock is shifted to sample the data. When the clock transitions, the actual data that is sampled is the data that was on the input pins a few hundred ps earlier. A graphical explanation of these timings is shown in the *Figure 4* and shows a sampling window of 350 ps.



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FIGURE 4. Serializer Setup and Hold Time

## Serializer Register Programmability

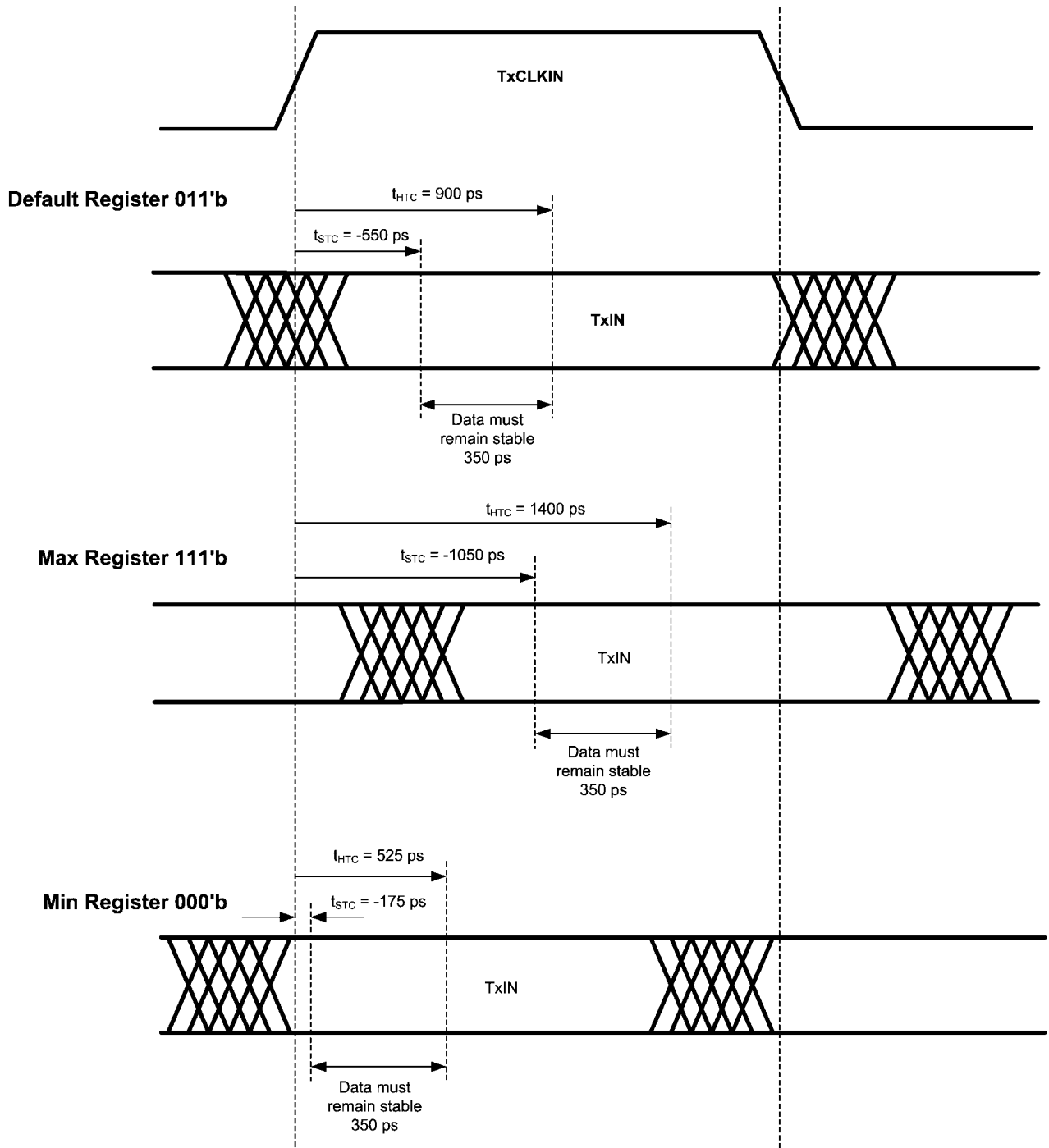
For the Serializer (LMH0340, LMH0040, LMH0050, and LMH0070) the clock to data delay can be optimized by programming register bits in the Serializer. This feature allows adjustment of the Serializer Setup and Hold time locations to be optimized to the Data Valid time provided by the FPGA host device.

To adjust the Serializer clock and data delay use register 0x30 bits [7:5]. The default delay between the clock and data is 725 ps (value 011'b). Each LSB changes the delay by 125 ps which gives a range in delay from 350 ps to 1225 ps.

See *Table 1* and *Figure 5*.

TABLE 1. Register 0x30 bits 7:5 Setup/Hold Delay Settings (\* = default)

Register Setting Reg 0x30 bits [7:5]	Sample Time Instant (ps)	Setup Time (ps)	Hold Time (ps)	Data Valid (ps)
000'b	350	- 175	525	350
001'b	475	- 300	650	350
010'b	600	- 425	775	350
<b>011'b *</b>	<b>725</b>	<b>- 550</b>	<b>900</b>	<b>350</b>
100'b	850	- 675	1025	350
101'b	975	- 800	1150	350
110'b	1100	- 925	1275	350
111'b	1225	- 1050	1400	350



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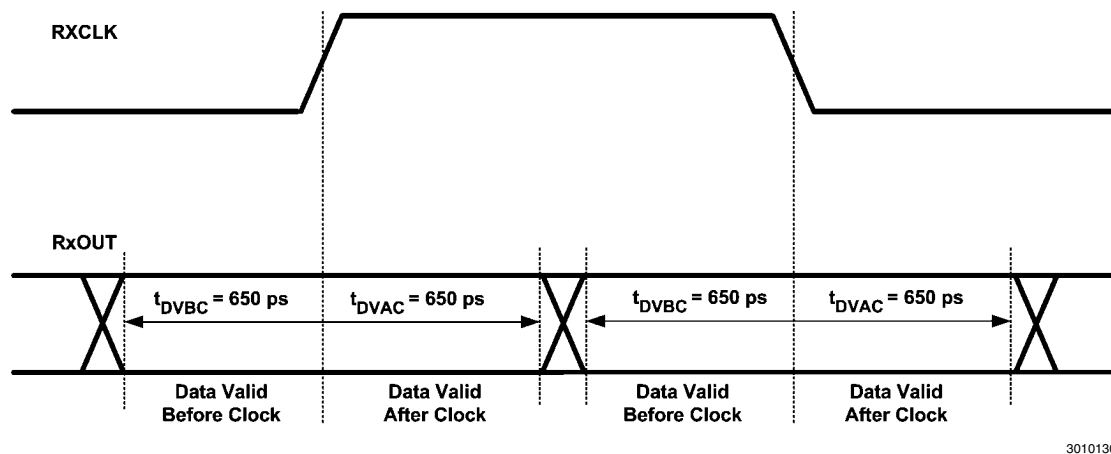
FIGURE 5. Clock and Data Phase Adjustment

## Deserializer Device Timing Requirements

For the Deserializers (LM0341, LMH0041, LMH0051 and LMH0071) the LVDS clock and data outputs are skewed to provide maximum setup and hold durations for the target FPGA. The Deserializer datasheet specifies  $t_{DVBC}$  and  $t_{DVAC}$

which specify the time during which the data is valid before and after the clock edge transition, centering the clock and data at a maximum line rate.

For example at a maximum line rate of 2.97 Gbps, the LVDS clock rate is 297 MHz or 3.4 ns. Divide this by 2 due to the DDR clocking and the data period is 1.7ns. This timing is shown in *Figure 6*.



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FIGURE 6. Deserializer (Setup and Hold Time) Data Valid Times

## Deserializer Register Programmability

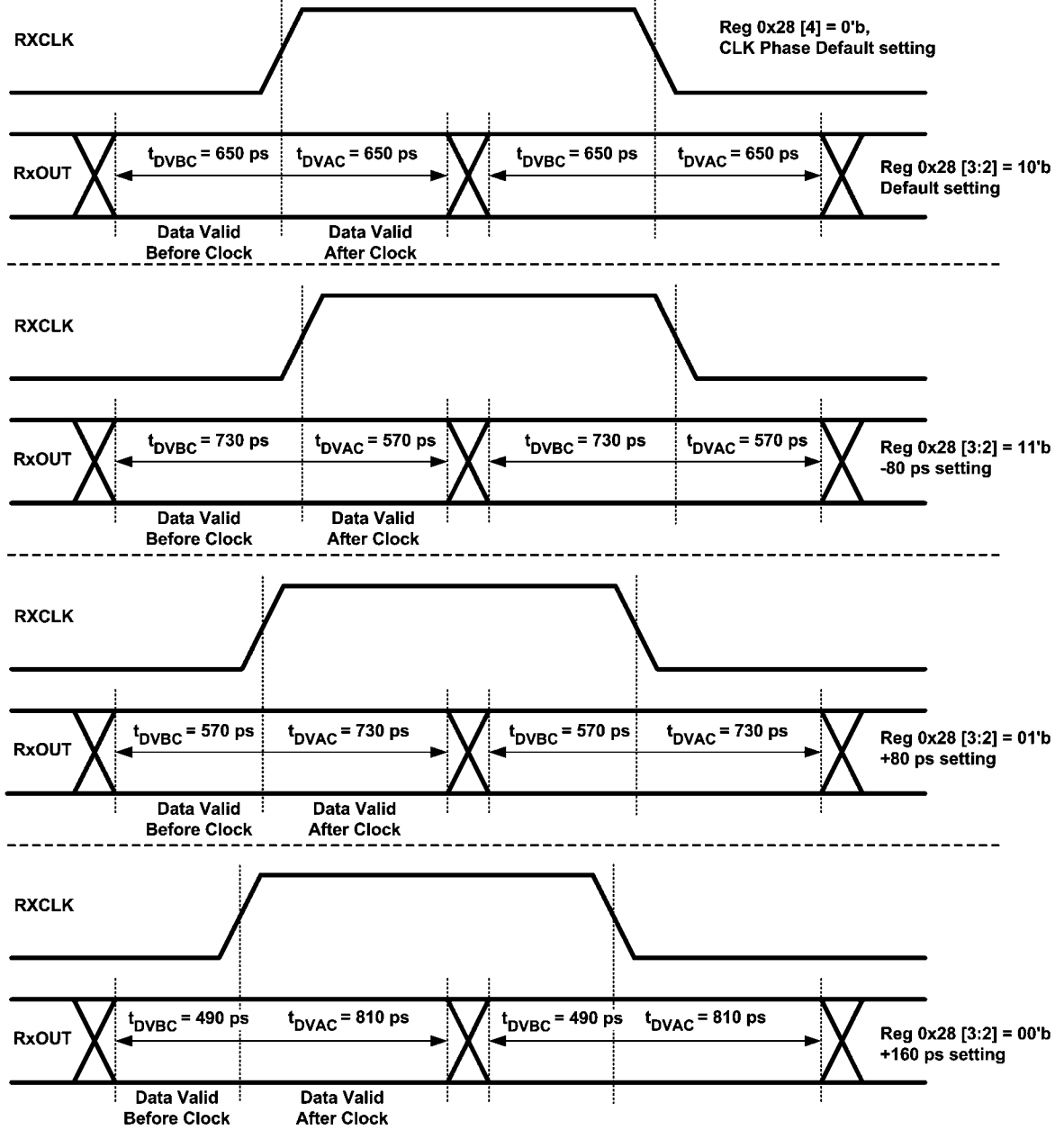
Like the Serializer, the Deserializer can also be optimized to adjust the clock edge location to be compatible with the downstream device's input timing requirement. To adjust the Deserializer, use register 0x28. Bits 2 and 3 of register 0x28

adjust the phase in 80 ps steps which gives 240 ps adjustment. The default value of register 0x28 is 10'b for an 800 ps setup and hold time. The time can be adjusted to a minimum of 640 ps and a maximum of 880 ps. The Data Valid After Clock (Hold) can be set from 960 ps to 720 ps.

The clock phase can also be inverted by bit 4 of register 0x28. See *Table 2* and *Figure 7*.

TABLE 2. Deserializer Clock and Data Phase Offset Settings Register 0x28 bits [3:2] (\* = Default)

Register Setting Reg 0x28 bits [3:2]	Offset (ps)	Data Valid Before Clock (ps)	Data Valid After Clock (ps)
00'b	160	490	810
01'b	80	570	730
<b>10'b *</b>	<b>0</b>	<b>650</b>	<b>650</b>
11'b	- 80	730	570



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FIGURE 7. Deserializer (Setup and Hold Time) Data Valid Times Programmability

## Conclusion

In summary, the DDR timing of the FPGA-Attach Serializers and Deserializers have been optimized for use with low cost FPGAs. Further, adjustability of the delay between the clock and data allows the user to configure the sampling window or the clock edge to optimize it for specific FPGA requirements.

## Referenced Parts

This application note refers to LMH0340, LMH0040, LMH0050, LMH0070, LMH00341, LMH00041, LMH00051 and LMH00071.

## Notes

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Serial Digital Interface (SDI)	<a href="http://www.national.com/sdi">www.national.com/sdi</a>	Mil/Aero	<a href="http://www.national.com/milaero">www.national.com/milaero</a>
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