

LM3668 Evaluation Board

National Semiconductor
Application Note 1623
Anne Lu
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Introduction

The LM3668 evaluation board is a working demonstration of a synchronous buck-boost DC-DC converter. This application note contains information about the evaluation board. For more details and electrical characteristics about the converter operation, please refer to the datasheet.

Operating Range

- V_{IN} range: 2.5V to 5.5V
- For 2.8V/3.3V and 3.0V/3.4V versions:
 - 1A maximum load current for $V_{IN} = 2.8V$ to 5.5V
 - 800mA maximum load current for $V_{IN} = 2.7V$
 - 600mA maximum load current for $V_{IN} = 2.5V$
- For 4.5V/5V version:
 - 1A maximum load current for $V_{IN} = 3.9V$ to 5.5V
 - 800mA maximum load current for $V_{IN} = 3.4V$ to 3.8V
 - 700mA maximum load current for $V_{IN} = 3.0V$ to 3.3V
 - 600mA maximum load current for $V_{IN} = 2.7V$ to 2.9V

Package

LLP-12 no-pullback (3mm x 3mm x 0.8mm)

Typical Application

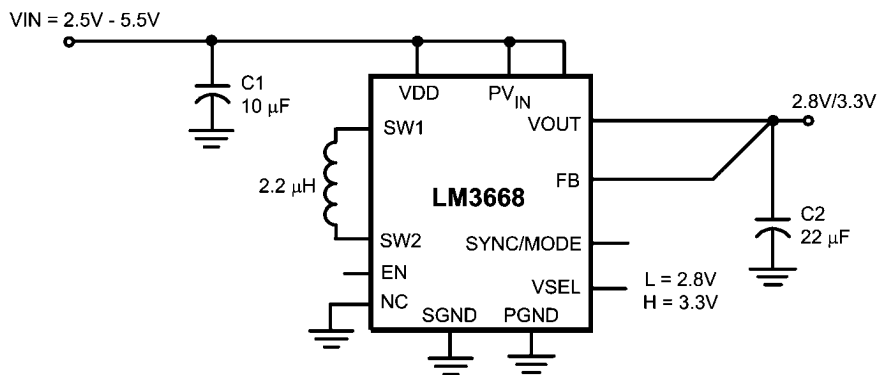
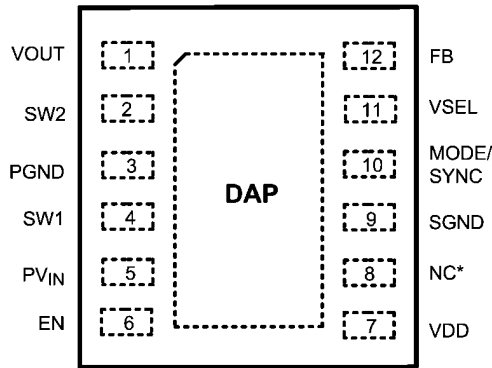


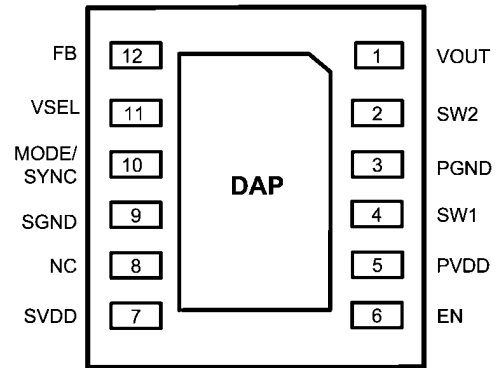
FIGURE 1. Typical Application Circuit

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Connection Diagrams



30018502



30018503

Note: the above figures are not to any actual scale

Pin Descriptions

Pin #	Pin Name	Description
1	VOUT	Connect to output capacitor.
2	SW2	Switching Node connection to the internal PFET switch (P2) and NFET synchronous rectifier (N2).
3	PGND	Power Ground.
4	SW1	Switching Node connection to the internal PFET switch (P1) and NFET synchronous rectifier (N1).
5	PV _{IN}	Supply to the power switch, connect to the input capacitor.
6	EN	Enable Input. Set this digital input high for normal operation. For shutdown, set low.
7	VDD	Signal Supply input. If board layout is not optimum an optional 1µF ceramic capacitor is suggested as close to this pin as possible.
8	NC	No connect. Connect this pin to SGND on PCB layout.
9	SGND	Analog and Control Ground.
10	MODE/SYNC	Mode = LOW, Automatic Mode. Mode= HI, Forced PWM Mode SYNC = external clock synchronization from 1.6MHz to 2.7MHz (When SYNC function is used, device is forced in PWM mode).
11	VSEL	Voltage selection pin; (i.e., 2.8V/3.3V option) Logic input low = 2.8V and logic high = 3.3V to set output Voltage.
12	FB	Feedback Analog Input. Connect to the output at the output filter.
DAP	DAP	Die Attach Pad, connect the DAP to SGND on PCB layout to enhance thermal performance. It should not be used as a primary ground connection.

Ordering Information

Order Number	Package	NSC Package Marking	Supplied As
LM3668SD - 2822	LLP-12	S016B	1000 units, Tape and Reel
LM3668SDX - 2833			4500 units, Tape and Reel
LM3668SD - 3034	LLP-12	S018B	1000 units, Tape and Reel
LM3668SDX - 3034			4500 units, Tape and Reel
LM3668SD - 4550	LLP-12	S019B	1000 units, Tape and Reel
LM3668SDX - 4550			4500 units, Tape and Reel

Note: As an example, if V_{OUT} option is 3.0V/3.4V, when V_{SEL} = Low, set V_{OUT} to 3V; when V_{SEL} = high, set V_{OUT} = 3.4V. This configuration applies to all voltage options.

Bill Of Materials

Component Name	Manufacturer	Specification	Case Size
LM3668SD	NSC	LLP-12	3mm x 3 mm x 0.8mm
$C_{IN} = 10\mu\text{F}$	Taiyo-Yuden	JMK212BJ106K	0805(2012)
$C_{OUT} = 22\mu\text{F}$ (2.8/3.3V, 3.0/3.4V)		JK212BJ226MG	0805(2012)
$C_{OUT} = 22\mu\text{F}$ (4.5/5.0V)		LMK212BJ226MMG	0805(2012)
$C_{IN-V_{DD}} = 4.7\mu\text{F}$		JMK212BJ475M	0805(2012)
Inductor	Coilcraft	LPS4018-222L	4mm x 4mm x 1.8mm

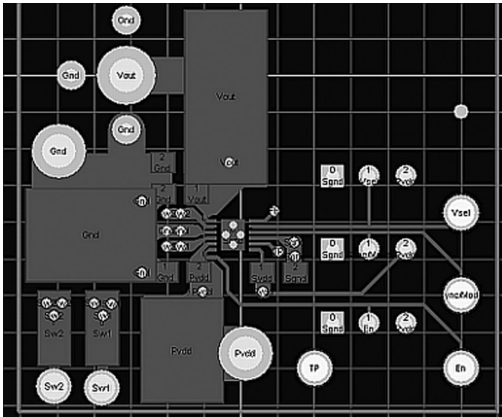
Operating Information

The LM3668 evaluation board is set for the following default positions:

- $V_{OUT} = 3.3V$, for $V_{OUT} = 2.8V$ move VSEL pin to Low via jumper
- SYNC Mode = H (PWM Mode), for Auto Mode, set SYNC = Low (move jumper to inner position). Do not leave this pin floating.
- EN pin is tied to V_{IN} via a jumper
- It is not recommended to start up the device with full load at minimum input voltage

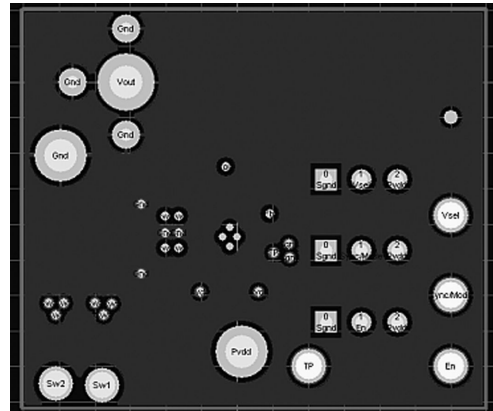
Evaluation Board Layout

LM3668EVB is a four-layer board designed to maximize the performance. Top layer consists of high current path; bottom layer is for low current and logic signals path. Inner layer 1 and layer 2 are dedicated for PGND (power GND) and SGND (analog and logic GND). For optimum performance, it is recommended to separate the PGND & SGND pins and join them together at the "star GND" on the PCB. The star GND traces on the PCB board should be close to the device power GND pin.



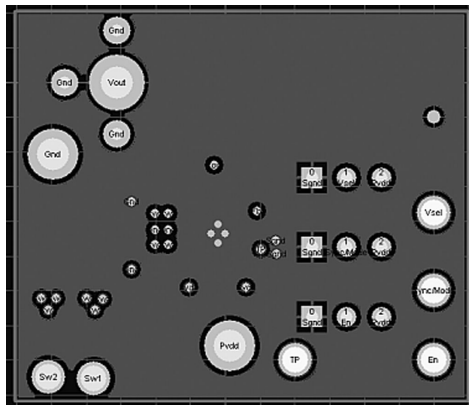
Top Layer

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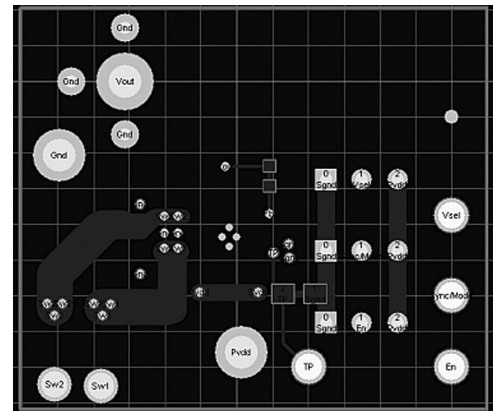
GND Inner Layer 1

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SGND Inner Layer 2

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Bottom Layer

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Notes

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Notes

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Switching Regulators	www.national.com/switchers	Distributors	www.national.com/contacts
LDOs	www.national.com/ldo	Quality and Reliability	www.national.com/quality
LED Lighting	www.national.com/led	Feedback/Support	www.national.com/feedback
Voltage Reference	www.national.com/vref	Design Made Easy	www.national.com/easy
PowerWise® Solutions	www.national.com/powerwise	Solutions	www.national.com/solutions
Serial Digital Interface (SDI)	www.national.com/sdi	Mil/Aero	www.national.com/milaero
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