

Simplified Programming of Altera FPGA's using a SCANSTA111/112 Scan Chain Mux

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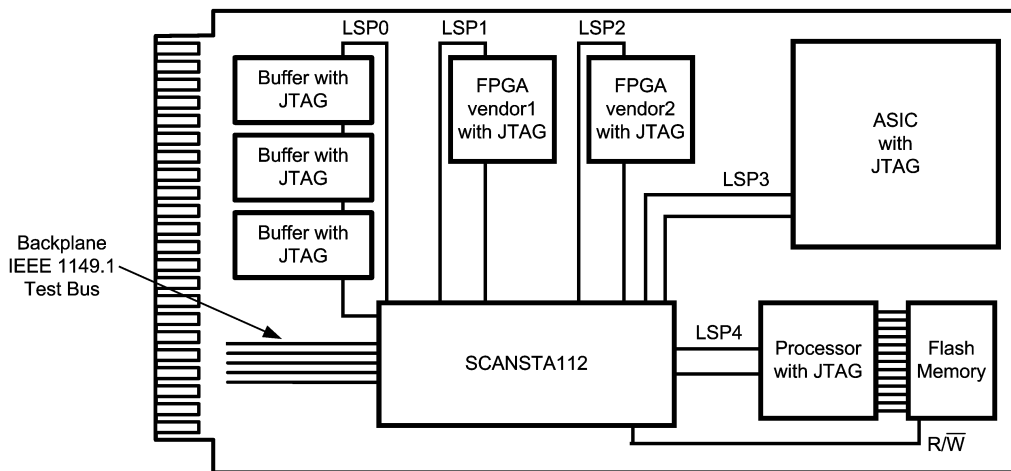
The SCANSTA111/112 Provides a Straightforward and Flexible Method of Isolating Scan Chains for Simplified Programming

Many modern communication and networking systems incorporate a system-wide IEEE 1149.1 (JTAG) test bus infrastructure. This test bus not only enables a comprehensive life-cycle approach to system test, but it also offers a number of additional benefits to the system designer as the utility of the JTAG bus continues to expand beyond the boundaries of just test. JTAG is now used for emulation, memory programming, and configuration of CPLD's or FPGA's, and these approaches are well supported by the industry.

As the JTAG test bus infrastructure expands within a circuit board or system, the need to manage the JTAG bus becomes apparent. Grouping similar technologies into smaller, local scan chains can reduce complexity and improve debug and fault isolation. Partitioning particular components onto an individual scan chain maximizes access for speed-critical applications, such as configuring large/multiple CPLD's or FPGA's. Systems with multiple cards and complex backplanes continue to utilize the JTAG infrastructure on each circuit card by extending the JTAG test bus across the backplane. Multiple cards can share the test bus when each card utilizes a JTAG interface device that enables multidrop JTAG.

National's SCANSTA111 and SCANSTA112 devices (STA11x) enable a backplane test bus and partitioning of scan chains. Each device supports a multidrop addressable backplane, and manages up to 3 or 7 local scan chains (respectively). The STA11x are commonly used for isolating components on a circuit board, particularly when configuring CPLD's or FPGA's.

When developing configuration vectors for Altera CPLD's, physically adding the STA11x into the scan path introduces a new device that the synthesis tool is not expecting. For some STA11x operating modes, the output of the synthesis tool, either JAM STAPL or SVF (Serial Vector Format), must be modified in order to access the target device through the STA11x. In order to configure the Altera device, there are a couple simple additional steps needed, and the following provides a basic description of how to accomplish this.



Typical use of SCANSTA112 to manage multiple JTAG chains on a single board

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SCANSTA111/112 Operating Modes

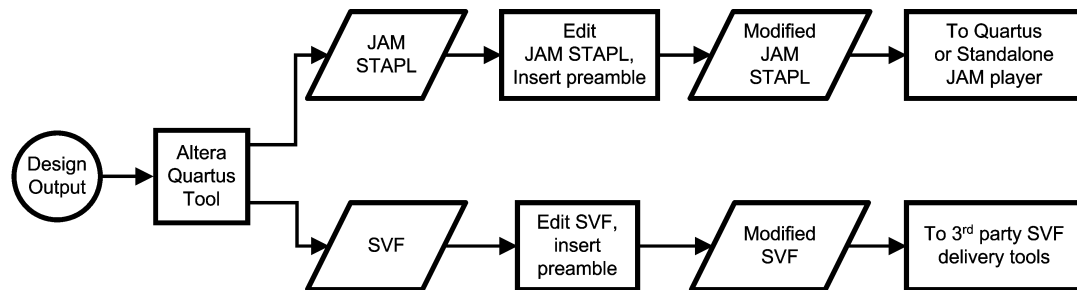
There are three basic ways to get "through" the STA11x devices: Transparent Stitcher Mode, Transparent ScanBridge Mode, and Normal ScanBridge mode.

Transparent Stitcher Mode (STA112 feature only) is activated by way of external pins, and does not require changes to the JAM STAPL or SVF, but does require external hardware control. SB/S = 0 selects the Stitcher mode, TRANS will put the device into transparent mode, and the LSP select pins are used to select the appropriate LSP.

Transparent ScanBridge Mode requires a preamble in the vectors that are used to configure the CPLD. The Quartus tool can provide a JAM STAPL file that may be modified to add the necessary preamble, and then the JAM STAPL may be played by the Quartus player, or by standalone JAM STAPL players. The Quartus tool can also write out an SVF file that can be "played" later by third party SVF delivery tools to do the actual configuration. Note that when the STA11x is in transparent mode it is simply buffering the dot1 signals. Therefore, it is adding delay and may require that the clock

speed be lowered. Examples 1 and 2 below demonstrate preambles to configure the STA11x device into Transparent ScanBridge Mode. Once this is executed, the STA11x device acts as a set of buffers between the backplane side and the LSP side of the device (i.e.; Tester TDO → STA11x TDI → STA11x LSP TDO → local chain → STA11x LSP TDI → STA11x TDO → Tester TDI).

Normal ScanBridge Mode also requires a preamble in the vectors used to configure an Altera CPLD. Note, however, that when the STA11x is not in transparent mode, it adds a re-synchronization bit (PAD-bit) to the end of the chain. This re-times the signals and allows for a clock speed equal to the original, but requires the addition of the pad bit into the scan path for each LSP inserted in the path. Examples 3 and 4 below demonstrate preambles to configure the device into normal ScanBridge Mode. Once this is executed, the STA11x acts as a set of buffers between the backplane side and the LSP side of the device, with the addition of the pad bits (i.e.; Tester TDO → STA11x TDI → STA11x LSP TDO → local chain → STA11x LSP TDI → PAD-bit → STA11x TDO → Tester TDI). Note that this will require additional bits in the scan process for the register and the pad-bits.



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Tool chain and process for modifying JAM STAPL or SVF

Example code from Altera Modified SVF

The following section of code is modified SVF from the Quartus tool output. In this example we have an STA11x device at hex address (1B) and the target device is located on LSP1. In the example below we have added two lines of code (lines 6 and 7) that address the correct device and select the correct local port.

```

!Device #01: XXXX - f:\work\svftest.pof
!NOTE "CHECKSUM" "02CC0FCAE";
TCK frequency: 10MHz
!
TRST ABSENT;
SIR 8 TDI(1B); ! <<<<-- level one protocol, STA11x at address 1B hex
SIR 8 TDI(A1); ! <<<<-- level two protocol, target device on LSP 1
ENDDR IDLE;
ENDIR IRPAUSE;
STATE IDLE;
SIR 10 TDI (044);
RUNTEST IDLE 10000 TCK ENDSTATE IDLE;
!
!CHECKING SILICON ID
!
SIR 10 TDI (042);
RUNTEST 50 TCK;
SDR 32 TDI (FFFFFFFF) TDO (41393800) MASK (FFFFFFFF00);
!
!
  
```

Example Code for Simulations and Verification

TRANSPARENT SCANBRIDGE MODE

For the first example, let's assume the STA11x is at address (11) and the target device is located on LSP0. In example 2, we assume the STA11x is at the same address but the target device is on LSP1.

Example 1: Configuring an LSP of the STA11x in Transparent ScanBridge mode.

```
TRST ON;
TRST OFF;
SIR 8 TDI (11); ! Select STA11x at slot address (11) (level 1 protocol)
SIR 8 TDI (a0); ! Load instruction to enable transparent mode for LSP0 (level 2 protocol)
SIR 8 TDI (a5); ! Verify SIR
SDR 8 TDI (5a); ! Verify SDR
SIR 8 TDI (c3); ! Try to load GOTOWAIT in STA11x
SDR 8 TDI (5a); ! Verify that STA11x did not recognize GOTOWAIT
! Now TDIB→lsp0→TDOB is the scan chain configuration
```

Example 2: Configuring an LSP of the STA11x in Transparent ScanBridge mode.

```
TRST ON;
TRST OFF;
SIR 8 TDI (11); ! Select STA11x at slot address (11) (level 1 protocol)
SIR 8 TDI (a1); ! Load instruction to enable transparent mode for LSP1 (level 2 protocol)
SIR 8 TDI (a5); ! Verify SIR
SDR 8 TDI (5a); ! Verify SDR
SIR 8 TDI (c3); ! Try to load GOTOWAIT in STA11x
SDR 8 TDI (5a); ! Verify that STA11x did not recognize GOTOWAIT
! Now TDIB→lsp1→TDOB is the scan chain configuration
```

NORMAL SCANBRIDGE MODE

For example 3, we assume the STA11x is at address (01) and LSP's 0, 1, and 2 will be connected to the backplane port. In example 4, we assume the STA11x is at the same address (01) but only LSP0 is connected to the backplane port.

Example 3: Configuring LSP's of the STA11x in "normal" ScanBridge mode.

```
TRST ON;
TRST OFF;
SIR 8 TDI (01); ! Select STA11x at slot address (01)
SIR 8 TDI (8e); ! modesel0 - Setup mode register 0 to select LSP 's
SDR 8 TDI (07); ! Set mode register bits 0,1,2 to select LSP0, LSP1, LSP2 of STA11x
SIR 8 TDI (e7); ! UNPARK to Sync LSPs to backplane port.
! MR0: X000X111
! Now TDIB→register→lsp0→pad→lsp1→pad→lsp2→pad→TDOB is the scan chain configuration
```

Example 4: Configuring LSP's of the STA11x in "normal" ScanBridge mode.

```
TRST ON;
TRST OFF;
SIR 8 TDI (01); ! Select STA11x at slot address (01)
SIR 8 TDI (8e); ! modesel0 - Setup mode register 0 to select LSP's
SDR 8 TDI (01); ! Set mode register bit 0 to select only LSP0 of STA11x
SIR 8 TDI (e7); ! UNPARK to Sync LSPs to backplane port.
! MR0: X000X001
! Now TDIB→register→lsp0→pad→TDOB is the scan chain configuration
```

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