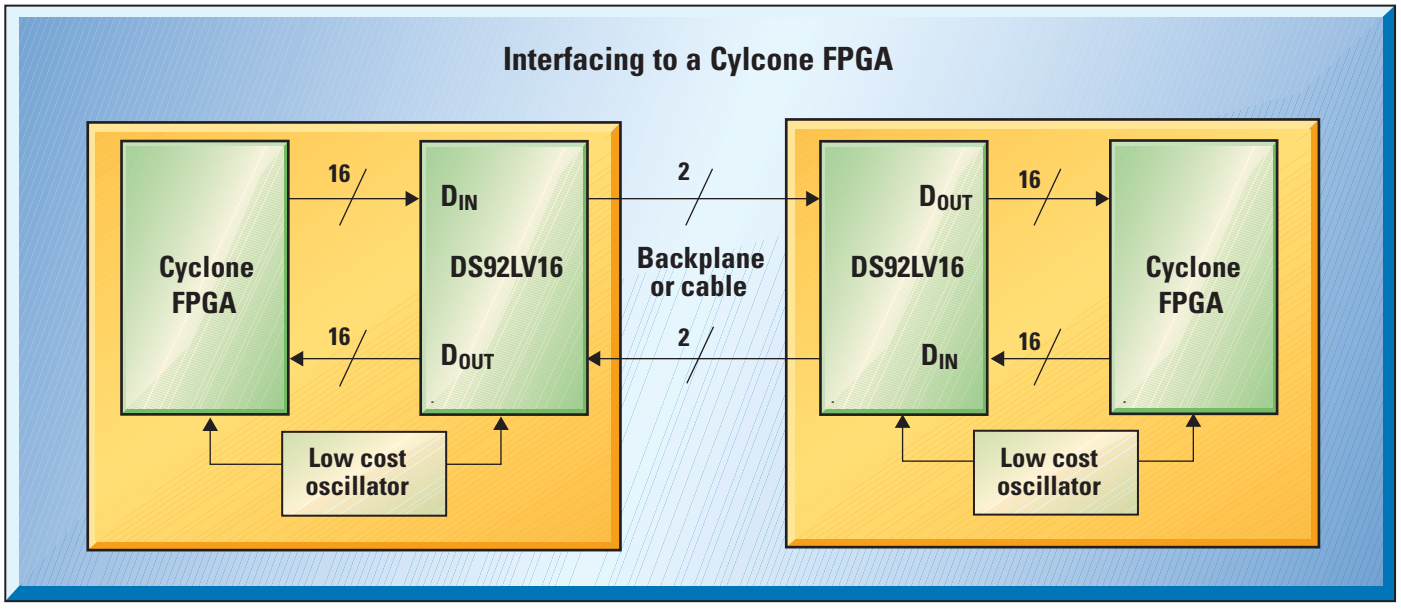
DS92LV16/18 Bus LVDS serializer/deserializer

For adding high-speed SerDes capability to FPGAs



Introduction

The DS9LV16/18 SerDes brings convenient high-speed serial communications capability to mid-range FPGAs such as the Altera Cyclone™ and MAX®II series without upgrading to a higher end family such as the Stratix™. The external SerDes increases bandwidth for mid-range FPGAs from 640 Mbps up to 1.28 Gbps, while improving signal reach and rate. It simplifies system design by reducing simultaneous switching noise (ground bounce) through lower I/O drive current and saves ground pins. This also results in reduced cost in terms of reduced PCB layers, cable width, and connector size and pins.

Product features

- DS92LV16- 25-80 MHz 16:1/1:16 serializer/deserializer 2.56 Gbps full duplex
- DS92LV18- 15-66 MHz 18:1/1:18 serializer/deserializer 1188 Mbps payload duplex
- Wide ±5% ref. clock frequency tolerance for relaxed transmitter and receiver clocking requirements
- Automatic receiver lock to random data allows true “plug and go” hot insertion capability without the need for special synchronization characters
- TIA/EIA-644 standard compliant LVDS interface
- Industrial temperature range -40 to 85°C
- Single 3.3V power supply
- Robust ESD protection 2.5 kV (DS92LV16), 2.0 kV (DS92LV18)
- Available in a compact PQFP-80 package

Applications

- High-speed industrial automation
- Networking- LAN and fixed access equipment
- Imaging and displays
- Broad market consumer

Sales tools

- Product brief
- Datasheet
- Design guide
- Cyclone FPGA application notes
- Evaluation board
- Ibis model

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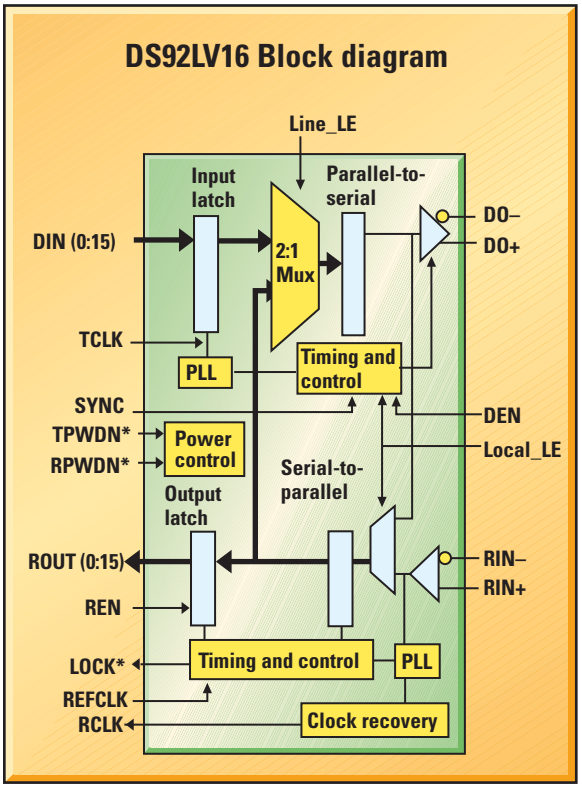
Product description

The DS92LV16 and DS92LV18 SerDes allow the user to send 16 bits and 18 bits respectively. The transmitter takes a 16 or 18 bit wide LVTTL bus and serializes it, embeds the clock, and transfers both onto one LVDS stream. The receiver takes a serial stream coming from another DS92LV16/18 and deserializes it onto a 16 or 18-bit bus and recovers the clock. The single serial stream simplifies transferring an 18 bit (or less) bus over PCB traces and cables by eliminating the skew problems between parallel data and clock paths. It saves system cost by narrowing data paths that in turn reduce PCB layers, cable width, connector size, and pins. The 18-bit payload of the DS92LV18 allows designers to send extra information such as parity, control bus, frame, etc.

The lock to random capability means there is no need to send special training characters or patterns, combined with the relaxed clocking requirements, the DS92LV18 is a more efficient system solution than most 8-bit or 10-bit SerDes solutions. In many cases, other systems require extra logic, more expensive clock distribution, and a much faster clock speed.

The DS92LV16/18 operates from a single 3.3V and consumes 104 mA (DS92LV16) and 90 mA (DS92LV18). They are available in compact LQFP-80 packages.



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