

Terms and Definitions for ADCs and DACs

This course discusses common terms and parameters used in discussing and testing ADCs and DACs. Emphasis is placed upon definitions of these terms and parameters. Many of these terms and parameters have been defined elsewhere, but this course serves as a single place to access these common terms.

Organization is alphabetical.

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Course Navigation

1.1 Course Navigation



Course Navigation

This course is organized like a book with multiple chapters. Each chapter may have one or more pages.

- The previous and next arrows move you forward and back through the course page by page.
- The left navigation bar takes you to any chapter. It also contains the bookmarking buttons, 'save' and 'go to.' To save your place in a course, press the 'save' button. The next time you open the course, clicking on 'go to' will take you to the page you saved or bookmarked.
- The 'Go to Final Test' button on the left navigation bar takes you back to the Analog University course listing, where you started. Take the course final test by clicking on 'Test Yourself.'
- The top services bar contains additional information such as glossary of terms, who to go to for help with this subject and an FAQ. Clicking home on this bar will take you back to the course beginning.
- Don't miss the hints, references, exercises and quizzes which appear at the bottom of some pages.



A - C

Terms beginning with letters "A" through "C".

- 2.1 Aliasing
- 2.2 Analog-to-Digital Converter (ADC)
- 2.3 Aperture Delay
- 2.4 Aperture Jitter
- 2.5 Bandwidth
- 2.6 Best Fit
- 2.7 Bit Error Rate (B.E.R.)
- 2.8 Coding Scheme
- 2.9 Common Mode Rejection Ratio (CMRR)
- 2.10 Common Mode Voltage
- 2.11 Conversion Time
- 2.12 Crosstalk



Aliasing

- **Aliasing** is the conversion of an input frequency to another frequency as a result of the conversion process.
- The output frequency of an ADC can never exceed $\frac{1}{2}$ the sampling frequency of the ADC without this being converted (aliased) to another frequency.
- **Aliasing** occurs when the input waveform is sampled at a rate less than **twice** the input waveform frequency.
- When the input frequency does exceed $\frac{1}{2}$ the sampling frequency, the output frequency becomes the absolute value of **[INT $(f_{IN}/f_S + 0.5) * f_S - f_{IN}$]**, where f_{IN} is the ADC input frequency and f_S is the ADC sample rate.
- **Aliasing** is a concern because, unless it is expected, can result in an **unexpected** and **possibly undesired** output frequency.

Aliasing



1 Aliasing is

1. Sampling at a rate less than twice the input frequency
2. The conversion of the input frequency to another frequency

3. An alternate name for the normal conversion process
4. Is never a concern when using an Analog-to-Digital Converter

1 Answer: 2 - The conversion of the input frequency to another frequency



2 To prevent aliasing, the sample rate must

1. Not exceed the input frequency.
2. Be greater than twice the highest input frequency.
3. Be less than twice the highest input frequency.
4. None of these is correct.

2 Answer: 2 - Be greater than twice the highest input frequency



Analog-to-Digital Converter (ADC)

- An **Analog-to-Digital Converter** is a circuit used to convert an analog input value into a digital output.
- There are **many ways** to convert an analog input into a digital output.
- The method used depends upon what is ultimately being accomplished, conversion rate needs, accuracy and resolution requirements, power requirements and cost factors.
- Common **conversion methods** include, but are not limited to, the following (in alphabetical order), with examples of National's products:
 - ▶ Delta-Sigma (or Sigma-Delta) - (ADC16061 [obsolete])
 - ▶ Flash - (none from National)
 - ▶ Folding and Interpolating (ADC08D1500)
 - ▶ Half-Flash - (ADC0820)
 - ▶ Integrating (slope) - (none from National)
 - ▶ Pipeline (ADC14L040)
 - ▶ Successive Approximation Register (SAR) - (ADC128S102)
 - ▶ Subranging - (ADC10D040)



Most of National's **high speed** ADCs use a pipeline architecture, while most of our **general purpose** ADCs use the successive approximation architecture.

Chapter 1



1 How many ways are there to do an analog to digital conversion?

1. One
2. Four
3. More than six
4. None of these is correct

1 Answer: 3 - More than six - - - - Eight examples were shown.



2 The method used to perform an analog to digital conversion depends upon

1. Conversion Rate needs

2. Accuracy needs
3. Both of these, and more
4. Neither of these is correct

2 Answer: 3 - Both of these, and more



3 Common ADC conversion methods include

1. SAR
2. Flash
3. Delta Sigma
4. All of these are common methods

3 Answer: 4 - All of these are common methods



4 Which of these ADC conversion methods is **NOT** used by any current National ADC

1. Subranging
2. Flash
3. Folding and Interpolating
4. None of these are used by any National ADC

4 Answer: 2 - Flash



5 Which conversion method (architecture) is used by most of our high speed ADCs?

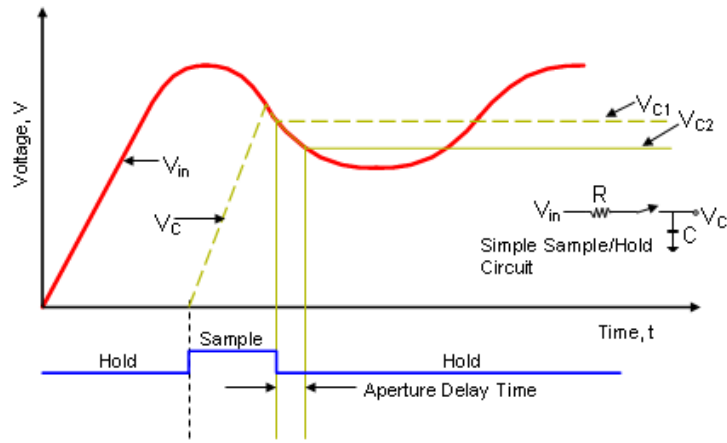
1. Flash
2. Half-Flash
3. Pipeline
4. Folding and Interpolating

5 Answer: 3 - Pipeline - - - - While our **highest speed** devices use the Folding and Interpolating architecture, the majority of our high speed devices are pipeline ones.



Aperture Delay

- **Aperture Delay** is the time delay after the edge of the sampling signal (often the input clock) for the sampling switch to open. The Sample/Hold circuit effectively stops capturing the input signal and goes into the "hold" mode the aperture delay after the specified signal edge.
- In the illustration here, V_{C1} would be acquired on the "hold" capacitor if **Aperture Delay** were zero. However, because of **Aperture Delay**, V_{C2} is actually held on the output "hold" capacitor.



Aperture Delay

Q

Aperture Delay is

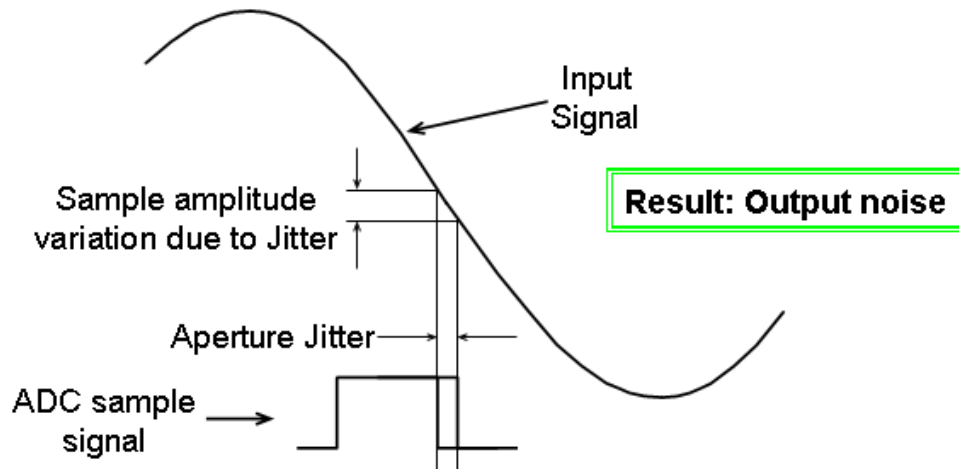
1. How long the aperture is open (how long the device is in the "sample" mode).
2. Rise time of the sampling signal.
3. Time delay in going into "hold" mode.
4. None of these is correct

1 Answer: 3 - Time delay in going into "hold" mode.

4.

Aperture Jitter

- Any sample-to-sample variation in aperture delay is **Aperture Jitter** or sampling jitter. Aperture jitter within the ADC can not be corrected or compensated for by the user.



- **Aperture Jitter** shows up as noise in the ADC output.
- The maximum jitter tolerable from all sources, from within the ADC and external to it, without affecting noise performance, is as indicated here, where t_j is the allowable rms jitter in seconds, V_{FS} is the peak-to-peak full scale input level, "n" is the ADC resolution in bits, "A" is the peak-to-peak input signal and f_{IN} is the signal input frequency.

$$t_j = \frac{V_{FS}}{2^{(n+2)} A \pi f_{IN}}$$

- Note that **sample rate** has **nothing** to do with the effects of aperture jitter.

Aperture Jitter

Q

1 Excessive aperture jitter shows up as noise in the ADC output

- True
- False

1 Answer: 1 - True

Q

2 The maximum jitter tolerable from all sources is a function of, among other things,

- Input Frequency
- Sample Rate
- Both of these
- Neither of these

2 Answer: 1 - Input Frequency

Q

3 Any sample-to-sample variation in Aperture Delay is known as

- Aperture Variation
- Questionable Aperture
- Aperture Jitter
- None of these is correct

3 Answer: 3 - Aperture Jitter

5.

Bandwidth

- Bandwidth** is the frequency range ($f_{MAX} - f_{MIN}$) over which a circuit will pass these frequencies with a specified limit to the output amplitude variation, assuming the input amplitudes of all frequencies are the same.
- Bandwidth** is generally specified to the -3 dB (power) level, but there is nothing saying that it can not be specified to some other level, higher or lower -3 dB.
- Bandwidth** can be specified as **Full Power Bandwidth** and as **Small Signal** Bandwidth.

Bandwidth

Q

1 Bandwidth is always

- Specified to the -3 dB level
- Measured from the full-scale level
- Both of these are correct
- Neither of these is correct

1 Answer: 4 - Neither of these is correct - - - - Answer "1" is generally but not always true for full power bandwidth. Answer "2" is not true for small signal bandwidth.



2 Bandwidth can be specified as

1. Full Power
2. Small Signal
3. Both of these are correct
4. Neither of these is correct

2 Answer: 3 - Both of these are correct



Best Fit

Best Fit is an INL test method

- The **Best Fit** method is one for testing INL where the transfer curve is compared with a straight line set to provide the best INL performance indication.
- This method provides a more conservative specification than does the "End Point" method.
- Justification for the **Best Fit** method includes the possibility of adjusting gain and offset to realize this high level of performance.
 - ▶ The problem with this justification is the fact that each circuit would require a separate adjustment, which might change over time and temperature.
- This method might actually be justified when only dynamic parameters are a concern and static errors, such as offset error and gain error, are of less concern.

Best Fit method.



1 The **best fit** method is one for

1. Determining the best architecture for a given application
2. Determining the ideal resolution for a given application
3. Testing INL
4. None of these is correct

1 Answer: 3 - Testing INL



2 The **Best Fit** method results in a more conservative INL specification than that provided by the **End Point** method.

1. True
2. False

2 Answer: 2 - False --- The Best Fit method results in a better spec, but the End Point method is more conservative



3 The "best fit" method

1. Is the best test method
2. Might sometimes be justified
3. Is completely useless
4. None of these is correct

3 Answer: 2 - Might sometimes be justified



Bit Error Rate (B.E.R.)

- **Bit Error Rate** (BER or B.E.R.) is the frequency at which a single bit error occurs.
- **Bit Error Rate** is actually a communications term and really should not be applied to data converters.
- For communications, **Bit Error Rate** is determined by dividing the number of individual bit errors by the product of the number of samples taken and the resolution (bits per word).
- As used with ADCs, **Bit Error Rate** is actually a **Word Error Rate** and can be described as the number of gross word errors divided by the number of samples taken.
- A high **Bit Error Rate** can be caused by a poor ADC design that results in "sparkle codes." Refer to the "sparkle code" definition.
- A better specification than **Bit Error Rate** for ADCs is *Sparkle Code Rate*, but this is typically not specified on ADC data sheets, either.

BER



Bit Error Rate is

1. Basically a communications spec.
2. Actually Word Error Rate in ADCs.
3. A spec that does not apply well to ADCs.
4. All of these are correct.

1 Answer: 4 - All of these are correct.



Coding Scheme

- An ADC **coding scheme** is the method used to determine which Input and Reference values become which Output Code. It is the **binary data format** used.
- A DAC **coding scheme** is the method used to determine which Input Code and Reference value becomes what analog output.
- The simplest coding scheme is **Straight Binary**.

Coding Scheme



1 An ADC coding scheme is

1. A way to build an ADC
2. The data format used
3. Both of these
4. Neither of these

1 Answer: 2 - The data format used - - - - A way to build an ADC would be its architecture.



2 An example of an ADC coding scheme is

1. Successive Approximation
2. Straight Binary
3. Both of these are examples
4. Neither of these is an example

2 Answer: 2 - Straight Binary - - - - "Successive Approximation" is an architecture.



3 The simplest coding scheme is

1. Straight binary
2. Grey code

- 3. Flash
- 4. Pipeline

3 Answer: 1 - Straight binary

9.

Common Mode Rejection Ratio (CMRR)

- **Common Mode Rejection Ratio** is a specification which applies to ADCs with differential inputs.
- **Common Mode Rejection Ratio** is a measure of how well the device tolerates a change in the common mode voltage without having the output change.

$$\text{CMRR} = \frac{\Delta \text{Output}}{\Delta V_{\text{CM}}}$$

- **Common Mode Rejection Ratio** is usually expressed in dB.



While conceptually a very simple specification, testing CMRR is not a trivial task.

Common Mode Rejection Ratio

Q

- 1 CMRR stands for
1. Common Mode Receive Ratio
 2. Common mode Rejection Rating
 3. Common Mode Rejection Ratio
 4. None of these is correct

1 Answer: 3 - Common Mode Rejection Ratio

Q

- 2 CMRR is specified for all ADCs
1. True
 2. False

2 Answer: 2 - False (Differential input ADCs only)

Q

- 3 Common Mode Rejection Ratio is a measure of
1. How well a device accepts a common mode signal
 2. How well the device tolerates a change in the common mode voltage without having the output change
 3. Either of these
 4. Neither of these is correct

3 Answer: 2 - How well the device tolerates a change in the common mode voltage without having the output change

10.

Common Mode Voltage

- **Common Mode Voltage** (V_{CM}) is the input voltage or current that is common to both pins of a differential pair.

- The imbalance within the differential circuit may cause the output to change some as the common mode voltage is changed.
- For inputs V_{IN+} and V_{IN-} ,

$$V_{CM} = [(V_{IN+}) + (V_{IN-})] / 2$$



1 Common mode voltage is

1. A common way of applying a voltage to two different circuits.
2. The input voltage that is common to both pins of a differential pair
3. A common way of designing an ADC input stage
4. None of these is correct

1 Answer: 2 - The d.c. input voltage that is common to both pins of a differential pair



2 The imbalance within the differential circuit may cause

1. The output to change as the common mode voltage changes
2. The output bits to become inverted
3. Both of these are correct
4. None of these is correct

2 Answer: 1 - The output to change as the common mode voltage changes



3 $[(V_{IN+}) + (V_{IN-})] / 2$ is what we call

1. V_{REF}
2. V_{CM}
3. Net V_{IN}
4. None of these

3 Answer: 2 - V_{CM}



Conversion Time

- **Conversion Time** is the time required to a complete a conversion.
- Since the **Conversion Time** does not include acquisition time, multiplexor set up time, or other elements of a complete conversion cycle, the conversion time is generally shorter than the time from the start of one conversion to the start of the next conversion.
- Sample rate is less than the inverse of **Conversion Time**.
- The **Conversion Time** is generally less than the Throughput Time.

Conversion Time



1 Conversion time is that time required

1. To do one complete conversion
2. From the start of one conversion to the start of the next conversion
3. Both of these are correct
4. Neither of these is correct

1 Answer: 1 - To do one complete conversion



2 Sample rate is

1. Less than the inverse of conversion time
2. The inverse of conversion time
3. Greater than the inverse of conversion time
4. None of these is correct

2 Answer: 1 - Less than the inverse of conversion time



3 Conversion Time includes acquisition time, multiplexor set up time, and other elements of a complete conversion cycle

1. True
2. False

3 Answer: 2 - False - - - - These times mentioned as included is *Throughput Time*



Crosstalk

- **Crosstalk** is the undesired coupling of energy from one channel or path to another.
- Because of capacitive and inductive coupling, energy from one channel on a die can find itself in another channel on the same die.
- The extent to which energy from one channel gets into another channel is called **Crosstalk**.
- Sometimes **Crosstalk** is so low that it is lost in the noise floor.
- When **Crosstalk** is within the noise floor, what we actually measure is noise and the actual **Crosstalk** is better than this.
- When **Crosstalk** is within the noise floor, for all practical purposes there is no crosstalk.

Crosstalk



1 The undesired coupling of energy from one channel or path to another is called

1. Intermodulation
2. Crosstalk
3. Interference
4. None of these is correct

1 Answer: 2 - Crosstalk



2 Energy from one channel on a die can find itself into another channel on the same die because of

1. Capacitive coupling
2. Inductive coupling
3. Both of these
4. None of these

2 Answer: 3 - Both of these



3 Sometimes crosstalk is so low (good) that it is lost in the noise floor

1. True
2. False

3 Answer: 1 - True



4 When crosstalk is so low (good) that it is lost in the noise floor

1. What we actually measure is noise
2. Cross talk is better than what we measure
3. Both of these
4. None of these

4 Answer: 3 - Both of these

D - E

Terms beginning with letters "D" and "E".

- 3.1 Differential Gain Error (DG)
- 3.2 Differential Linearity Error (DLE)
- 3.3 Differential Non-Linearity (DNL)
- 3.4 Differential Phase Error (DP)
- 3.5 Digital Feedthrough
- 3.6 Digital-to-Analog Converter (DAC)
- 3.7 Dynamic Applications
- 3.8 Dynamic Parameters
- 3.9 Effective Number of Bits (ENOB)
- 3.10 End Point



Differential Gain Error (DG)

- **Differential Gain Error** is the percentage difference between the output amplitudes of a specified small signal sine wave input at two different dc input levels.
- **Differential Gain Error** is primarily a video specification.
- It is unusual to find a **Differential Gain Error** specification on ADC or DAC data sheets, except for those intended for video applications.



The ADC1175 is an example of an ADC with a [Differential Gain Error](#) specification.

Differential Gain Error



1

The percentage difference between the output amplitudes of a specified small signal sine wave input at two different dc input levels is called

1. Bandwidth
2. Differential Gain Error
3. Small Signal Error
4. None of these is correct

1 Answer: 2 - Differential Gain Error



2 Differential Gain is a specification that is primarily for

1. Video applications
2. Audio applications

3. Both of these are correct
4. Neither of these is correct

2 Answer: 1 - Video applications



3 Differential Gain

1. Is a video specification
2. Is not found on all ADC data sheets
3. Both of these are correct
4. Neither of these is correct

3 Answer: 3 - Both of these are correct

2.

Differential Linearity Error (DLE)

- **Differential Linearity Error (DLE)** is the same as and is another name for **Differential Non-Linearity**.

Differential Linearity Error



Differential Linearity Error is another name for **Differential Non-Linearity**.

1. True
2. False

1 Answer: 1 - True

3.

Differential Non-Linearity (DNL)

- **Differential Non-Linearity (DNL)** is the measure of the *maximum* deviation from the ideal step size of 1 LSB.
- **Differential Non-Linearity** for a given step is equal to the actual size of that step in LSB minus the expected (1 LSB) step size.
- The **worst positive** and **worst negative** values are used for the DNL specification.
- **Differential Non-Linearity** is commonly measured at the rated clock frequency with a ramp input, but *can* be measured by comparing the digitized sine wave with a theoretically perfect sine wave.



A 3-bit converter with individual DNL errors of 0, -0.1, +0.2, -0.6, +0.4, -0.2, +0.2, +0.1, 0 LSB will have a DNL specification of +0.4 / -0.6 LSB because these are the worst positive and negative DNL values.

DNL



1 **Differential Linearity Error** and **Differential Non-Linearity** are different names for the same specification.

1. True
2. False

1 Answer: 1 - True



2 Subtracting the expected step size of 1 LSB from the actual step size gives us

1. DNL for that step

2. INL for that step
3. ILE for that step
4. None of these is correct

2 Answer: 1 - DNL for that step



3 The maximum difference between the ideal step size and 1 LSB is called

1. Integral Linearity Error (ILE)
2. Integral Non-Linearity (INL)
3. Differential Non-Linearity (DNL)
4. None of these is correct

3 Answer: 3 - Differential Non-Linearity (DNL)



4 The DNL specification is the

1. Lowest positive and lowest negative of all DNL values
2. Average of the positive and lowest negative of all DNL values
3. Worst positive and worst negative of all DNL values
4. None of these is correct

4 Answer: 3 - Worst positive and worst negative of all DNL values



5 DNL is commonly measured

1. At half the rated clock frequency
2. With an exponential input
3. Both of these are correct
4. Neither of these is correct

5 Answer: 4 - Neither of these is correct - - - DNL is commonly measured at the rated clock frequency with a ramp input.



Differential Phase Error (DP)

- **Differential Phase Error** is the difference in the output phase of a reconstructed small signal sine wave at two different dc input levels.
- **Differential Phase Error** is primarily a video specification.
- It is unusual to find a **Differential Phase Error** specification on ADC or DAC data sheets, except for those intended for video applications.



The ADC1175 is an example of an ADC with a Differential Gain Error specification.

Differential Phase Error



1 The difference in the output phase of a reconstructed small signal sine wave at two different dc input levels is called

1. Group Delay
2. Differential Phase Error
3. Phase Delay
4. None of these is correct

1 Answer: 2 - Differential Phase Error



2 Differential Phase is a specification that is primarily for

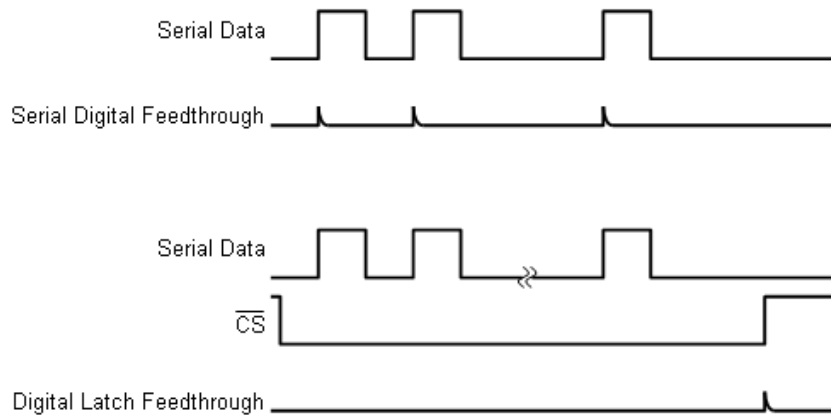
1. Video applications
2. Audio applications
3. Both of these are correct
4. Neither of these is correct

2 Answer: 1 - Video applications



Digital Feedthrough

- **Digital Feedthrough** is the energy that gets to the output of a DAC as a result of a change in the digital input code or upon the occurrence of a clock edge.
- **Digital Feedthrough** is the result of energy that gets through switches or other devices that are supposed to be turned off or provide isolation.



- An example of **Digital Feedthrough** is the perturbations that comes through to a DAC output on clock edges, or as data is loaded into an internal shift register or latch.
- DAC **Digital Feedthrough** produces output spikes that can be considered to be output noise.
- **Digital Feedthrough** is differentiated from **Glitch** or **Glitch Energy** in that **Digital Feedthrough** is the result of digital activity *at the DAC digital input pins* and **Glitch Energy** is the result of *internal digital word update*.

Digital Feedthrough



1 Digital feedthrough causes

1. DAC output noise
2. DAC output spikes
3. Both of these are correct
4. Neither of these is correct

1 Answer: 3 - Both of these are correct



2 Digital Feedthrough occurs as a result of a change in digital data

1. True
2. False

2 Answer: 1 - True

6.

Digital-to-Analog Converter (DAC)

- A **Digital-to-Analog Converter (DAC)** is a circuit used to convert a digital input word to an analog output.
- There are a lot of ways to construct a DAC. The type of DAC used depends upon what is ultimately being accomplished, update (conversion) rate needs, accuracy and resolution requirements, power requirements and cost factors.
- DAC converter types include (but are not limited to):
 - ▶ R / 2R Ladder
 - ▶ Resistor String
 - ▶ Segmented
 - ▶ Switched Capacitor



Like an ADC, a DAC must have a reference.

The DAC

Q

1 The type of DAC used depends upon

1. Update (conversion) rate needs
2. Accuracy and resolution requirements
3. Power requirements
4. All of the above

1 Answer: 4 - All of the above

Q

2 A **Digital-to-Analog** Converter

1. Converts an **analog (input) quantity** into a **digital word**
2. Does not need a reference
3. Both of these are correct
4. Neither of these is correct

2 Answer: 4 - Neither of these is correct - - - - A DAC has a **digital input and analog Output**; all converters need a reference.

7.

Dynamic Applications

- **Dynamic Applications** are those circuit applications where **dynamic signals** are processed, as opposed to applications where slowly changing d.c. voltages are processed.
 - ▶ **Dynamic Applications** of ADCs are characterized by having an a.c. signal at the ADC input.
 - ▶ **Dynamic Applications** of DACs are characterized by having an a.c. signal at the DAC output.
- **Dynamic Applications** examples include communications/radio signal processing, music, audio, vibration analysis.

Dynamic Applications



1 Dynamic applications are those

1. Whose function changes from time to time
2. Where a.c. signals are processed
3. That use a randomly changing reference
4. None of these is correct

1 Answer: 2 - Where a.c. signals are processed



2 An application where a DAC is used to trim a bias level is an example of a dynamic application

1. True
2. False

2 Answer: 2 - False - - - - This would be a static application.



3 Examples of dynamic applications include

1. Communications signal processing
2. Vibration analysis
3. Both of these
4. Neither of these

3 Answer: 3 - Both of these



Dynamic Parameters

- **Dynamic Performance Parameters** are those parameters that describe how the device performs in an environment where the analog signal (ADC input or DAC output) is an a.c. signal as opposed to a static or slowly moving d.c. voltage.
- Examples of **Dynamic Performance Parameters** are SNR, THD, SINAD, ENOB, SFDR, IMD and Crosstalk.

Dynamic Performance Parameters



1 Dynamic Performance parameters are those that describe how the device performs in an environment where the

1. Reference is continually changing
2. Analog signal is an a.c. one
3. Either of these
4. Neither of these

1 Answer: 2 - Analog signal is an a.c. one



2 Examples of dynamic performance parameters include

1. ENOB
2. DNL
3. INL
4. All of these

2 Answer: 1 - ENOB - - - - DNL and INL are static parameters



9.

Effective Number of Bits (ENOB)

- **Effective Number of Bits** (ENOB) is another method of specifying **Signal-to-Noise and Distortion Ratio**, or **SINAD**.
- **ENOB** is defined as $(\text{SINAD} - 1.76) / 6.02$ and says that the converter is equivalent to a perfect ADC of this (ENOB) number of bits.
- Because **SINAD** is derived from **SNR** and **THD** and **ENOB** is a direct calculation from SINAD, ENOB will depend upon **SNR** and **THD**.



While SNR dominates SINAD and using SNR or SINAD to calculate ENOB will yield figures close to each other, it is really not correct to use SNR to calculate ENOB, although some converter suppliers do so for some devices.

ENOB



1 Effective Number of Bits is another way of specifying

1. Resolution
2. SNR
3. SINAD
4. None of these is correct

1 Answer: 3 - SINAD - - - - ENOB is calculated directly from SINAD



2 ENOB is defined as

1. $(6.02 \times n) / \text{SINAD}$
2. $(\text{SNR} - 1.76) / 6.02$
3. $(\text{SINAD} - 6.02) / 1.76$
4. None of these is correct

2 Answer: 4 - None of these is correct - - ENOB = $(\text{SINAD} - 1.76) / 6.02$



3 ENOB will depend upon SNR and THD

1. True
2. False

3 Answer: 1 - True - - - - ENOB is calculated from SINAD, which is a combination of SNR and THD



End Point

- The **End Point** method for testing INL compares the transfer curve to a straight line between the end points of the transfer curve.
- Compare the **End Point** and **Best Fit** INL test methods.
- The **End Point** INL test method is more conservative than is the **Best Fit** method.
- The INL of a converter that uses the **End Point** INL test method should not be compared with the INL of a converter that uses the **Best Fit** INL test method as there is no correlation between the methods.

End Point



1 The **End Point** Method is one for determining

1. The ADC input values corresponding to zero scale and full scale
2. The DAC output values corresponding to zero scale and full scale
3. INL

4. Both 1 and 2 are correct

1 Answer: 3 - INL

Q 2

The INL of a converter that uses the End Point method should **not** be compared with one that uses the Best Fit method.

1. True
2. False

2 Answer: 1 - True - - - - The methods are not compatible or comparable

F - G

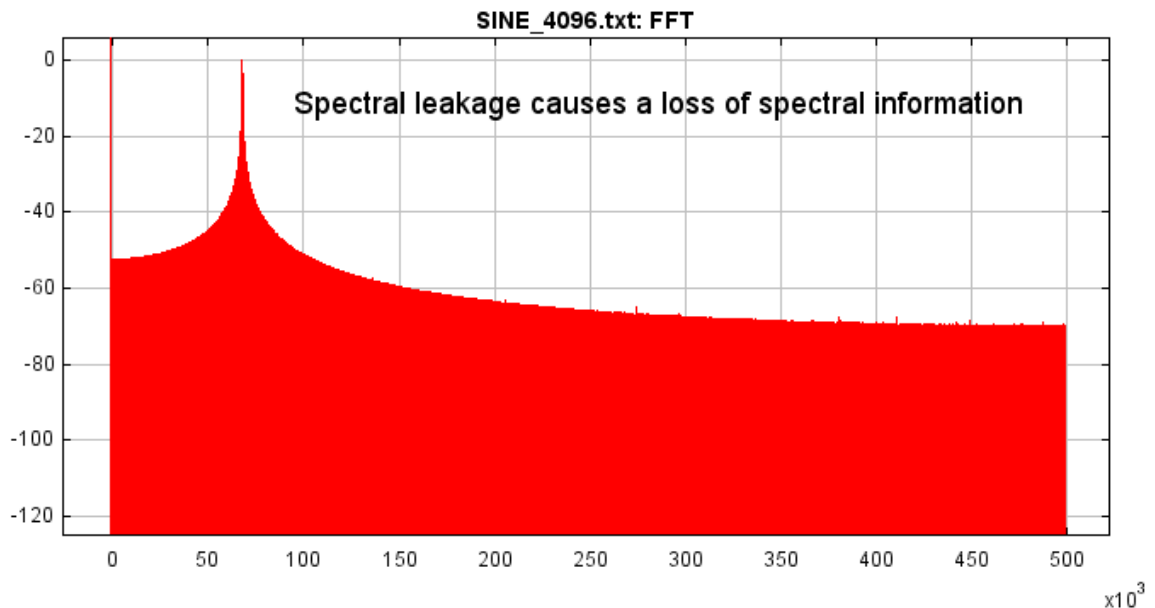
Terms beginning with letters "E" and "G".

- 4.1 Fast Fourier Transform (FFT)
- 4.2 Frequency Domain Plot
- 4.3 Full Power Bandwidth
- 4.4 Full Scale Error
- 4.5 Full Scale Input Range
- 4.6 Full Scale Recovery Time
- 4.7 Gain Error
- 4.8 Gain Error Tempco
- 4.9 Gain Factor
- 4.10 Glitch Energy

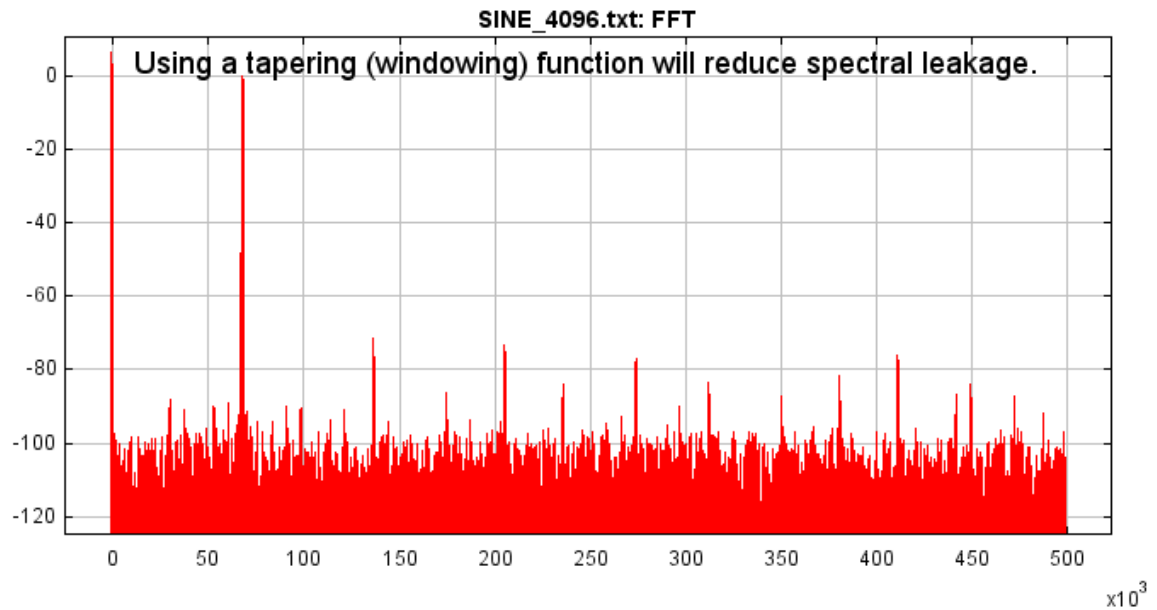
1.

Fast Fourier Transform (FFT)

- The **fast Fourier transform** (FFT) is a discrete Fourier transform (DFT) algorithm which reduces the number of computations needed for N points from $2 \times N^2$ down to $2 \times N \times \text{LOG}_2(N)$, where LOG_2 is the base-2 logarithm.
- The **Fourier transform** is the method used to convert time domain signals in to the frequency domain and vice-versa.
- If the function to be transformed is **not harmonically related** to the sampling frequency, the response of an FFT looks like a *sinc function*, giving us **spectral leakage** (although the integrated power is still correct).



- **Spectral leakage** can be reduced by using a **tapering function**. However, spectral leakage reduction by tapering is accomplished at the expense of decreasing the spectral resolution.



- ▶ **Tapering** is more commonly known as **Windowing**.



Unlike the DFT, the FFT requires a radix 2 number of samples. That is, the number of samples must be 2 to the power of an integer.

FFT



1 The fast Fourier transform requires

1. Fewer computations than does the discrete Fourier transform
2. A radix 2 number of samples
3. Both of these are correct
4. Neither of these is correct

1 Answer: 3 - Both of these are correct



2 Converting signals from the time domain to the frequency domain

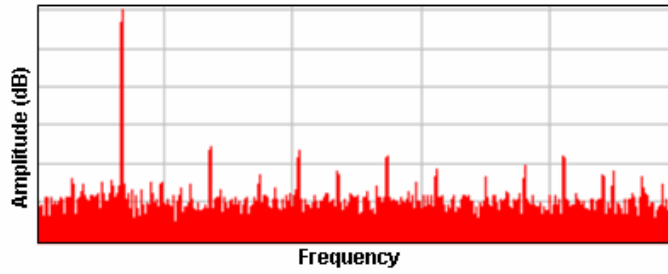
1. Requires the use of a Fourier transform
2. Can be done, but is not practical
3. Can not be done
4. None of these is correct

2 Answer: 1 - Requires the use of a Fourier transform



Frequency Domain Plot

- A **Frequency Domain Plot**, commonly called an **"FFT"** or **"FFT Plot"**, is a plot that shows the frequency content of a signal.
- A **Frequency Domain Plot** is a plot of amplitude vs. frequency.



Frequency Domain Plot

Q

A Frequency Domain Plot is

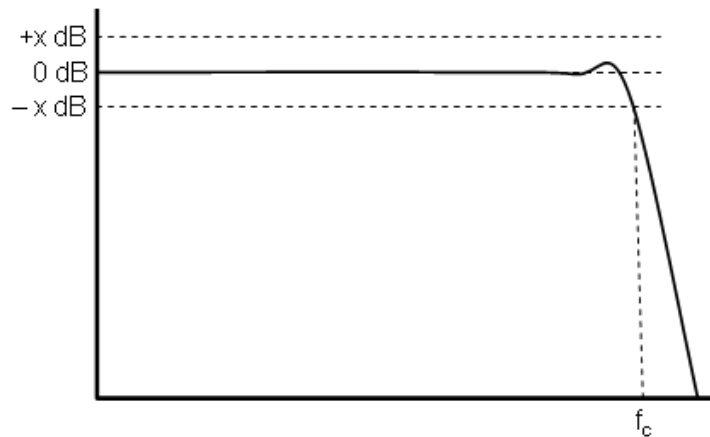
1. Commonly called an "FFT"
2. A plot of amplitude vs. frequency
3. Both of these are correct
4. Neither of these is correct

1 Answer: 3 - Both of these are correct

3.

Full Power Bandwidth

- **Full Power Bandwidth** is the frequency range over which the reconstructed output signal amplitude remains within a given range when there is a full scale input.



- This "given range" is **usually** 3 dB, but sometimes we may see a different range specified.

Full Power Bandwidth

Q

Full Power Bandwidth is always the 3 dB bandwidth.

1. True
2. False

1 Answer: 2 - False

4.

Full Scale Error

- **Full Scale Error** is a measure of how far the last code transition is from the ideal transition point.
- The ideal full scale transition point is **1.5 LSB** below the nominal full scale point.
- **Full Scale Error** is defined as:

$$V_{FSE} = V_{max} + 1.5 \text{ LSB} - G \times V_{REF}$$

where V_{max} is the voltage at which the transition to the maximum code occurs and is expressed in Volts. The 1.5 LSB and V_{REF} are in the same units. "G" is the converter gain factor.



Full Scale Error is a measure of how far the last code transition is from the ideal transition point.

1. True
2. False

1 Answer: 1 - True



Full Scale Input Range

- **Full Scale Input Range** (FSR) of an ADC is the input range of voltages (or currents) over which the ADC will digitize that input without going under range or over range.
- **Full Scale Input Range** is defined as follows, where "**S**" = 1 for an ADC with a single-ended input and "**S**" = 2 for an ADC with a differential input. For the case where the ADC has a differential input, the FSR is the **Differential** input.

$$FSR = S \times G \times REF$$

- From the above formula we see that FSR can be increased by increasing the reference.
- If the peak-to-peak input signal goes beyond the Full Scale Input Range, the output will be clipped.

Full Scale Input Range



1 A 12-bit, differential input ADC with a gain factor (G) of unity and a 2.00V reference with a 3.5V_{P-P} input signal

1. Has a Full Scale Differential Input Range of 1.00V
2. Has a Full Scale Differential Input Range of 2.00V
3. Will have a clipped output.
4. None of these is correct.

1 Answer: 4 - None of these is correct - - - - Full scale Differential Input Range of twice the reference voltage. Clipping occurs when the input peak-to-peak input goes beyond the full scale range.



2 Full Scale Input Range

1. Increases with reference voltage.
2. Is the range without clipping.
3. Both of these are correct.
4. Neither of these is correct.

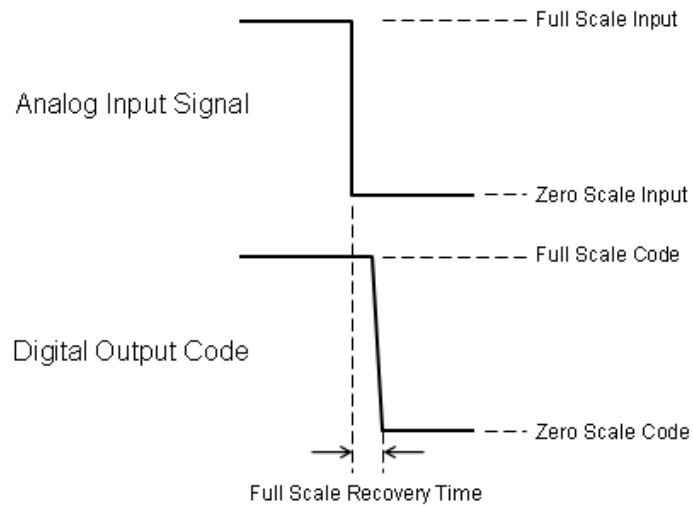
2 Answer: 3 - Both of these are correct.



6.

Full Scale Recovery Time

- **Full Scale Recovery Time** is the time required after the input makes a step from one input extreme to the other and settles sufficiently for the converter to recover and make a conversion with its rated accuracy.



- **Full Scale Recovery Time** should not be confused with **Over Range Recovery Time**.

Full Scale Recovery Time



Full Scale Recovery Time and **Over Range Recovery Time** are the same thing.

1. True
2. False

1 Answer: 2 - False



Gain Error

- **Gain Error** is the deviation from the ideal slope of the transfer function.
- For **single-ended** inputs, **Gain Error** can be calculated as:

$$\text{Gain Error} = \text{Full Scale Error} - \text{Offset Error}$$

For **differential** inputs, **Gain Error** can be calculated as:

$$\text{Gain Error} = \text{Positive Full Scale Error} - \text{Negative Full Scale Error}$$

Gain Error



Gain Error can be calculated from

1. Full Scale Error and Offset Error for single-ended converters.
2. Positive and Negative Full Scale Errors for differential converters.
3. Both of these are correct.
4. Neither of these is correct.

1 Answer: 3 - Both of these are correct.

8.

Gain Error Tempco

- **Gain Error Temperature Coefficient** is a measure of how much the gain error changes with temperature.
- **Gain Error Temperature Coefficient** is usually expressed in parts per million per degree Celsius (ppm/°C).

Gain Error Temperature Coefficient

Q

Gain Error Temperature Coefficient

1. Is a useless spec that tells us nothing.
2. Is usually expressed in parts per million per degrees Celsius.
3. Both of these are correct.
4. Neither of these is correct.

1 Answer: 2 - Is usually expressed in parts per million per degrees Celsius.

9.

Gain Factor

- **Gain Factor** is a multiplier for the effective value of the reference.
- **Gain Factor** is assumed to be unity, unless otherwise stated.

Gain Factor

Q

Unless otherwise stated, gain factor is assumed to be

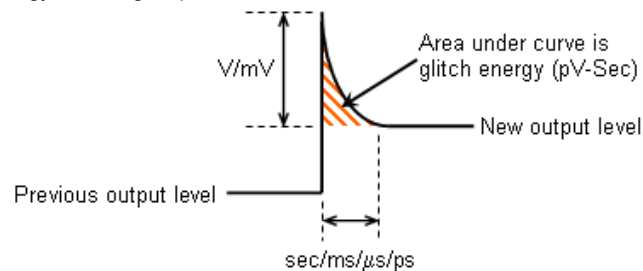
1. Undefined
2. Zero
3. Unity
4. None of these is correct

1 Answer: 3 - Unity

10.

Glitch Energy

- **Glitch Energy** is the energy in the signal perturbation or disturbance that occurs at the DAC output when the input code is updated.



- **Glitch Energy** is worst at the **major carry**. See definition of "major carry".
- **Glitch Energy** should not be confused with **Digital Feedthrough**.

Glitch Energy



Glitch Energy and *Digital Feedthrough* are actually the same thing.

1. True
2. False

1 Answer: 2 - False

I - L

Terms beginning with letters "I" through "L".

- 5.1 Integral Linearity Error (ILE)
- 5.2 Integral Non-Linearity (INL)
- 5.3 Intermodulation Distortion (IMD)
- 5.4 Jitter
- 5.5 Least Significant Bit (LSB)



Integral Linearity Error (ILE)

- **Integral Linearity Error (ILE)** is another term for **Integral Non-Linearity (INL)**.
- These are two terms for the same, identical specification.

ILE



INL and ILE are two names for the same, identical specification.

1. True
2. False

1 Answer: 1 - True



Integral Non-Linearity (INL)

- **Integral Non-Linearity (INL)** is a specification that describes the deviation of the ADC or DAC transfer curve from a straight line.
- **Integral Non-Linearity** defines the bow in the transfer curve.
- **Integral Non-Linearity** describes the extent to which the transfer curve is not linear.
- The worst positive and worst negative values are used for the INL specification.
- There are two methods of measuring INL: **End Point** and **Best Fit**.

INL



1 INL describes the

1. Deviation of the ADC or DAC transfer curve from a straight line
2. Extent to which the transfer curve is not linear.
3. Both of these are correct
4. Neither of these is correct

1 Answer: 3 - Both of these are correct

Q

2 INL is determined by

1. Averaging all of the readings
2. Taking the worst positive and negative readings
3. Calculating the root sum square of all readings
4. None of these is correct

2 Answer: 2 - Taking the worst positive and negative readings

Q

3 The *End Point* and *Best Fit* methods of determining INL are compatible with each other.

1. True
2. False

3 Answer: 2 - False

3.

Intermodulation Distortion (IMD)

- **Intermodulation Distortion** is the ratio of the power in the *intermodulation products* to the power in one of the original input frequencies.
- *Intermodulation products* can be created when two or more sinusoidal frequencies are applied to the ADC input at the same time.
- The **third order** intermodulation products are generally the most important ones.
 - ▶ The second order intermodulation products are $(f_1 + f_2)$ and $(f_1 - f_2)$
 - ▶ The third order intermodulation products are $(2 \times f_1 + f_2)$, $(f_1 + 2 \times f_2)$, $(2 \times f_1 - f_2)$ and $(2 \times f_2 - f_1)$.
 - ◆ Since the second order intermodulation products tend to be far from the carrier, they are easily filtered out and are usually of little concern.
 - ◆ Because the third order intermodulation products tend to fall close to the carrier, they are of most concern.
- **Intermodulation Distortion** is usually expressed in dB.

Intermodulation Distortion

Q

1 Intermodulation distortion can result

1. When two or more frequencies are applied to an ADC input at the same time
2. From circuit nonlinearities
3. Both of these are correct
4. Neither of these is correct

1 Answer: 3 - Both of these are correct

Q

2 Intermodulation products farthest from the carrier are of most concern.

1. True
2. False

2 Answer: 2 - False

4.

Jitter

- **Jitter** is the variation in the position of a point on a periodic waveform, or the placement of the rising or falling edge of a digital signal.
- **Jitter** can also be the variation in the duty cycle of a periodic waveform.
- Converter clock **Jitter** will degrade the converter noise performance.
- **Jitter** is usually specified in rms units.
- **Jitter** in the *time domain* is **phase noise** in the *frequency domain*.

Jitter



1 Excessive jitter can cause a degradation in SNR performance

1. True
2. False

1 Answer: 1 - True



2 Jitter is usually specified in peak-to-peak units.

1. True
2. False

2 Answer: 2 - False - - - - Jitter is usually specified in rms units.

5.

Least Significant Bit (LSB)

- The **Least Significant Bit** (LSB) is the bit (binary digit) of a digital word that has the smallest value or weight.
- The **Least Significant Bit** value is $G \times V_{REF}/2^n$ where "**G**" is the reference gain factor (which is most often unity) and "**n**" is the converter resolution in bits.

Least Significant Bit



The value or weight of the Least Significant Bit is

1. $V_{REF}/(G \times 2^n)$.
2. $G \times V_{REF}/2^n$.
3. $V_{REF}/2^n$.
4. None of these is correct.

1 Answer: 2 - $G \times V_{REF}/2^n$.

M - O

Terms beginning with letters "M" through "O".

- 6.1 Major Carry
- 6.2 Missing Code
- 6.3 Mixed Signal Device

- 6.4 Monotonic
- 6.5 Monotonicity
- 6.6 Most Significant Bit (MSB)
- 6.7 Multiplying DAC
- 6.8 Multiplying DAC Solution
- 6.9 Offset Error
- 6.10 Output Delay
- 6.11 Output Hold Time
- 6.12 Over Range Recovery Time

1.

Major Carry

- The **Major Carry** of a digital word is where the code changes from a **0** followed by all ones to a **1** followed by all zeros.
- Typically, the worst error for both DACs and ADCs are at the **major carry**.
- Sometimes we hear the plural, **Major Carries**, which refers to, in addition to the **Major Carry** as previously described, refers to the code changes from a **00** followed by all ones to a **01** followed by all zeros, and sometimes also to where the code changes from a **000** followed by all ones to a **001** followed by all zeros.

Major Carry



The point where a digital code goes from a **0** followed by all ones to a **1** followed by all zeros is called the

1. Middle Code
2. Trouble Code
3. Major Carry
4. None of these is correct

1 Answer: 3 - Major Carry

2.

Missing Code

- A **Missing Code** is a code that can never appear at the output of the ADC.
- A **Missing Code** cannot be reached with any input value.
- One or more codes will be **missing** when the negative DNL is -1.0 .

Missing code



A missing code is

1. One that a DAC will not accept
2. One that can not appear at the ADC output
3. Not likely with a DNL more negative than -1.0
4. None of these is correct

1 Answer: 2 - One that can not appear at the ADC output

3.

Mixed Signal Device

- A **Mixed Signal Device** is one that has both Analog and Digital functions on a single die.
- **Mixed Signal Devices** include ADCs and DACs.
- **Mixed Signal Devices** also include microprocessors that have an ADC and/or DAC on the die and ASICs that have both analog and digital functions.

Mixed Signal



1 An example of a mixed signal device includes the

1. ADC
2. DAC
3. Both of these are examples
4. Neither of these is an example

1 Answer: 3 - Both of these are examples



2 Mixed signal devices includes

1. Microprocessors with an ADC on the die
2. ASICs with both analog and digital functions
3. Both of these
4. Neither of these

2 Answer: 3 - Both of these



Monotonic

- The word **Monotonic** indicates a condition where the slope of the transfer function has a constant sign.
- This term is generally used to describe a **DAC**.
- If a **Non-Monotonic DAC** is used to build an **ADC**, that ADC will have one or more **missing codes**.

Monotonic/Monotonicity



Monotonicity

1. Is a condition where the transfer function slope has a constant sign
2. Is used to describe DACs
3. Both of these
4. Neither of these

1 Answer: 3 - Both of these



Monotonicity

- **Monotonicity** is "Having the quality of being monotonic." It is a condition where the transfer function has a constant sign.
- That is, a Monotonic device has a transfer function whose slope direction does not change.
- **Monotonicity** is a term used to describe DACs with this characteristic.
- **Monotonicity** is not generally used to describe **ADCs**.

Monotonicity

Q 1

A DAC given a code sequence of 08h, 09h, 0Ah, 0Bh, 0Ch. If the DAC is monotonic, which of the following (rounded off) output sequences are possible?

1. 163mV, 170mV, 178mV, 186mV, 194mV
2. 31mV, 35mV, 39mV, 43mV, 47mV
3. Both of these are possible
4. Neither of these is possible

1 Answer: 3 - Both of these are possible - - - - The **only** requirement for monotonicity is that the output does not reverse direction unless the input code reverses direction.

Q 2

With the same input code sequence in the above question, an output sequence of 31mV, 35mV, 39mV, 39mV, 45mV indicated a non-monotonic DAC.

1. True
2. False

2 Answer: 2 - False - - - - There is no reversal of direction in the transfer function, even though two adjacent codes are the same.

6.

Most Significant Bit (MSB)

- The **Most Significant Bit** is the bit that has the *largest value* or weight.
- The value of the **Most Significant Bit** is *one half of full scale*.

MSB

Q

The value of the MSB is

1. $2^n / n$
2. Half of full scale
3. Full scale / 2^n
4. None of these is correct

1 Answer: 2 - Half of full scale

7.

Multiplying DAC

- A **Multiplying DAC** is one that can accommodate a wide range of reference voltages or currents, which are allowed to be an a.c. signal.
- A **Multiplying DAC** may be used as *digital attenuator*.
- To use a **Multiplying DAC** as a *digital attenuator*, the signal to be controlled is applied to the reference input. The output is then described as indicated here, where "G" is the DAC gain factor and "D" is the analog equivalent of the digital input word.

$$\text{Output Amplitude} = \frac{G \times D \times \text{Input Amplitude}}{2^n}$$



The DAC0800 is an example of a multiplying DAC.

Offset Error

Q 1

A single-ended ADC has an ideal transition to the first code of 1.024mV, but the actual first code transition occurs at 1.280mV. The Offset Error of this ADC is

1. A positive value.
2. A negative value.
3. 1/2 LSB
4. None of these is correct.

1 Answer: 1 - A positive value - - - - This is because the actual transition point is more positive than the ideal transition point. We can not say what the error is without knowing the DAC resolution.

Q 2

With an input code of **00h**, a 10-bit DAC with a 2.0 Volt reference and $G = 1$ has an output voltage of 3.0 mV with an ideal output in this case of 0.0 mV. The Offset Error in this case

1. Can not be determined with the information given.
2. Is 3.0 mV.
3. Is 1.5 mV.
4. None of these is correct.

2 Answer: 2 - Is 3.0 mV - - - - The difference between the actual and expected output values when the input code is zero is defined as the offset error, which, in this case, is 3.0 mV

10.

Output Delay

- **Output Delay** (t_{OD}) of an ADC is the time delay after the edge of the input clock or other specified signal before the data update is present at the output pins.
- **Output Delay**, together with **Output Hold Time**, is used to determine which clock or other signal edge is best used to latch the output data.

Output Delay

Q

Output Delay (t_{OD}) and Output Hold Time (t_{OH}) are the same thing.

1. True
2. False

1 Answer: 2 - False - - - - If they were the same thing, we would not use **both** of them to determine which clock or other signal edge is best used to latch the output data.

11.

Output Hold Time

- **Output Hold Time** is length of time that the output data is valid after the edge of the input clock or **other specified signal**.
- Together with **Output Delay**, the **Output Hold Time** is used to determine which clock or other signal edge is best used to latch the output data.

Output Hold Time

Q

Which of these is used to determine which clock or other signal edge is best used to latch the output data?

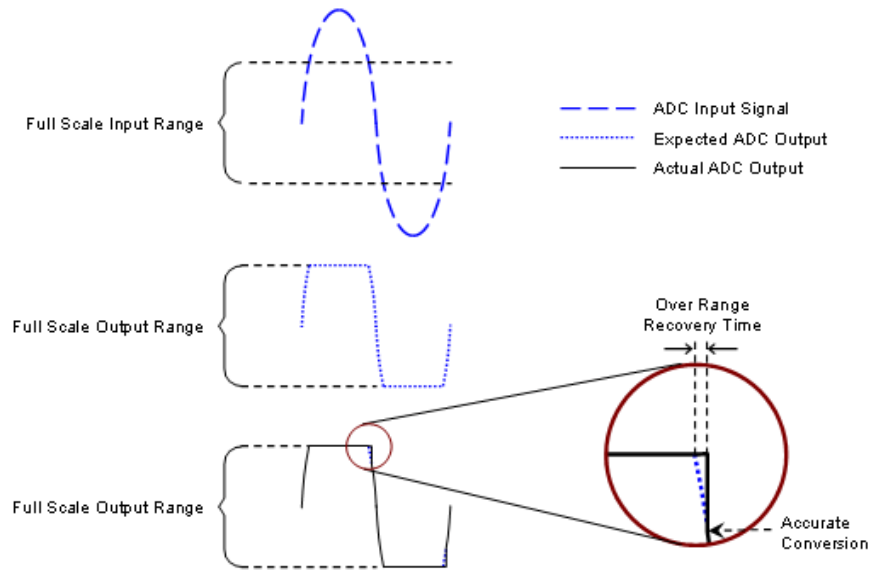
1. Output Delay (t_{OD}).
2. Output Hold Time (t_{OH}).
3. Both of these are used.
4. Neither of these is used.

1 Answer: 3 - Both of these are used.

12.

Over Range Recovery Time

- **Over Range Recovery Time** is the time required after V_{IN} goes from a specified level outside of the normal input range to a specified voltage (or current) within the normal input range and the converter makes a conversion with its rated accuracy.



- **Over Range Recovery Time** should not be confused with **Full Scale Recovery Time**.

Over Range Recovery Time

Q

Full Scale Recovery Time and Over Range Recovery Time are the same thing.

1. True
2. False

1 Answer: 2 - False - - - - Full Scale Recovery Time considers a *full scale* signal and Over Range Recovery Time considers a signal that goes **beyond full scale**.

P - Q

Terms beginning with letters "P" and "Q".

- 7.1 Pipeline Delay
- 7.2 Power Supply Rejection Ratio (PSRR)
- 7.3 Quantum
- 7.4 Quantization
- 7.5 Quantization Error
- 7.6 Quantization Noise
- 7.7 Quantization Uncertainty
- 7.8 Quantizer

1.

Pipeline Delay

- **Pipeline Delay** is the number of clock cycles between initiation of conversion and when the data for that conversion is presented to the output driver stage.
- Data for any given sample is available the **Pipeline Delay** plus the **Output Delay** after that sample is taken.
- New data is available at every clock cycle, but the data lags the acquisition by the **Pipeline Delay** plus the **Output Delay** (t_{OD}).
- Most, but not all, high speed ADCs exhibit some **pipeline delay**.

Pipeline Delay

Q

1 Having a pipeline delay means that the ADC will require more than one clock cycle for each output word.

1. True
2. False

1 Answer: 2 - False - - - - Having a pipeline delay means that **any given** sample result is available a specified number of clock cycles after that sample is taken, NOT whether there is more than one cycle per sample or conversion.

Q

2 All high speed ADCs exhibit some pipeline delay

1. True
2. False

2 Answer: 2 - False - - - - The flash converter does not have a pipeline delay.

2.

Power Supply Rejection Ratio (PSRR)

- **Power Supply Rejection Ratio** can be one of two specifications.
 - ▶ **D.C. PSRR** is the ratio of the change in a specified parameter (e.g., Full Scale Error) that results from a specified change in the power supply voltage.
 - ◆ **D.C. PSRR** says *nothing* about how well noise on the power supply is rejected.
 - ▶ **AC PSRR** is measured with a signal of specified frequency and amplitude riding upon the power supply and is the ratio of the output amplitude of that signal at the output to its amplitude on the power supply pin.
- Most National Semiconductor ADCs specify both **A.C. PSRR** and **D.C. PSRR**
- Products from our competition generally specify only **A.C. PSRR**
- PSRR is usually specified in dB.



We normally assume that PSRR is AC PSRR, but data sheets (for data converters, amplifiers, etc.) most often only specify what we here call DC PSRR

PSRR

Q

1 There is only one way to specify PSRR.

1. True
2. False

1 Answer: 2 - False - - - - There are at least two ways.

Q 2 Most products from most suppliers that specify PSRR, including but not limited to ADCs and amplifiers, specify

1. A.C. PSRR
2. D.C. PSRR
3. Both of these
4. Neither of these

2 Answer: 2 - D.C. PSRR

Q 3 Most National Semiconductor ADCs specify

1. A.C. PSRR
2. D.C. PSRR
3. Both of these
4. Neither of these

3 Answer: 3 - Both of these

3.

Quantum

- A **Quantum** is the magnitude of the *range of ADC input values* that is assigned a single digital code.

$$\text{Quantum} = \frac{G \times V_{\text{REF}}}{2^n}$$

- While we sometimes see the use of the word **Quanta** (plural) to indicate this range, since this range is a single one, it is more appropriately called a **Quantum** (singular).

Quantum

Q

A Quantum is

1. A Range of input values assigned a single code
2. 2^n
3. Both of these
4. Neither of these

1 Answer: 1 - A Range of input values assigned a single code

4.

Quantization

- **Quantization** is the process of digitizing, or of assigning a single digital code to a range of input values (a quantum).

Quantization

Q

Quantization is

1. Digitization
2. Determining the size of a Quantum
3. Both of these are correct

4. Neither of these is correct

1 Answer: 1 - Digitization - - - - This is by definition. The size of a Quantum (LSB) is determined by the ADC resolution, reference value and gain factor.

5.

Quantization Error

- **Quantization Error** is the error that results from the quantization (digitization) process.
- Since it is the result of the digitization (quantization) process, **Quantization Error** can not be reduced to zero.

Quantization Error

Q

Since it results from the quantization process, quantization error can not be reduced to zero.

1. True
2. False

1 Answer: 1 - True

6.

Quantization Noise

- **Quantization Noise** is the ADC noise that results from the quantization (digitization) process.
- **Quantization Noise** is also the floor below which we can never reduce the noise and is a function of the ADC resolution.
- **Quantization Noise** can be reduced by increasing the resolution.

Quantization Noise

Q

1 Because it results from the quantization process, quantization noise can not be reduced to zero.

1. True
2. False

1 Answer: 1 - True

Q

2 Quantization Noise is reduced by

1. Increasing the reference voltage or current
2. Increasing the resolution
3. Both of these
4. Neither of these

2 Answer: 2 - Increasing the resolution - - - - Increasing the reference **increases** quantization noise

7.

Quantization Uncertainty

- When looking at the digital code of an ADC output, we know that any input within a *range* of input values (a *quantum*) could have produced that code and we are *uncertain* as to the exact input value that produced that code, so we have a degree of "uncertainty" as to what the input value was that produced the output code.

- **Quantization Uncertainty** is what we call this uncertainty due to the quantization process.
- **Quantization Uncertainty** can be reduced by increasing ADC resolution, but can never be reduced to zero.

Quantization Uncertainty

Q

1 Quantization Uncertainty

1. Can not be reduced to zero
2. Results from the quantization process
3. Both of these are correct
4. Neither of these is correct

1 Answer: 3 - Both of these are correct

Q

2 Quantization Uncertainty can be reduced by

1. Increasing the reference
2. Increasing the resolution
3. Both of these are correct
4. Neither of these is correct

2 Answer: 2 - Increasing the resolution

8.

Quantizer

- A **Quantizer** is a device which quantizes its input.
- An Analog-to-Digital converter is a **Quantizer**.

Quantizer

Q

An ADC is a Quantizer.

1. True
2. False

1 Answer: 1 - True - - - - - By definition

R - S

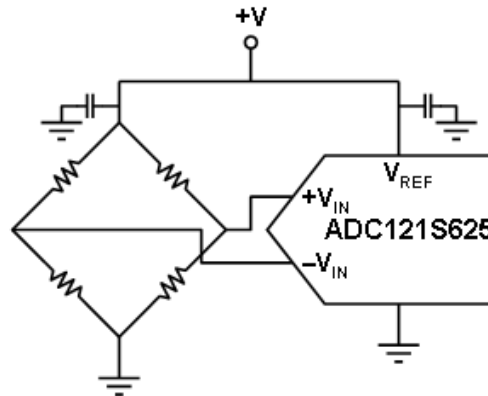
Terms beginning with letters "R" and "S".

- 8.1 Ratiometric Operation
- 8.2 Reference
- 8.3 Resolution
- 8.4 Settling Time
- 8.5 Signal-to-Noise and Distortion (SINAD)
- 8.6 Signal-to-Noise Ratio (SNR)
- 8.7 Small Signal Bandwidth
- 8.8 Sparkle Codes
- 8.9 Spectral Leakage
- 8.10 Spectral Resolution
- 8.11 Spurious Free Dynamic Range (SFDR)

1.

Ratiometric Operation

- When the same voltage source is used for both for the ADC reference and as excitation source for a transducer or signal source connected to the ADC input, the ratio of the output of that transducer or signal source to the reference remains constant, regardless of changes in that voltage source.
- The ADC output code is a function of the ratio of the signal source output to the reference voltage and, for a limited reference voltage range, the ADC output code is independent of the value of that reference voltage.
- **Ratiometric Operation** of an ADC is the use of a common (the same) voltage source for the ADC reference voltage and to excite or bias the transducer connected to the input.



An example of ratiometric operation

Ratiometric Operation



Ratiometric operation makes, for a limited reference range, conversion result independent of reference value

1. True
2. False

1 Answer: 1 - True

2.

Reference

- All data converters use a **Reference**.
- All data converters have both a top and a bottom reference voltage (or current).
 - ▶ The top and bottom reference voltages may be called V_{REF+} and V_{REF-} , V_{RT} and V_{RB} , V_{RP} and V_{RN} or any number of other designations. With each of those designations shown here, the first one must be more positive than the other one.
 - ▶ In all cases the upper reference inputs must be higher than the lower reference.
 - ▶ The upper reference is often called the *positive* reference and the lower reference is often called the *negative* reference.
 - ▶ When referring to the reference voltage inputs, "positive" and "negative" only indicate relative polarity and not necessarily positive and negative voltages or currents.
- If we assume the reference is a voltage, the total (or net) reference voltage is the upper reference voltage minus the lower reference voltage.
- Assuming reference pins to be labeled as V_{REF} , the **net reference voltage** is

$$V_{REF} = V_{REF+} \text{ minus } V_{REF-}$$

This is the what the ADC considers its reference voltage to be.

- Sometimes the reference may be internally generated, or may be the supply voltage,
- For an **ADC**, the *Reference* is the *voltage* or *current* against which the analog input is compared to determine the digital output code.
- For a **DAC**, the *Reference* is the *voltage* or *current* that is used as a multiplier for the digital input code to determine the output voltage or current.

Reference



1 Unlike ADCs, DACs do not need a reference.

1. True
2. False

1 Answer: 2 - False - - - - **All** DACs and ADCs need a reference.



2 All data converters have a top and a bottom reference.

1. True
2. False

2 Answer: True - - - - Sometimes the lower reference is ground and can not be changed.



3 Assuming a reference voltage, the total reference voltage is

1. The top (positive) reference
2. The sum of the top and the bottom references
3. The difference between the top and bottom references
4. None of these is correct

3 Answer: 3 - The difference between the top and bottom references



4 Assuming a reference voltage, the upper reference voltage must always be more positive than the negative reference voltage.

1. True
2. False

4 Answer: 1 - True



Resolution

- There are two definitions of **resolution**:
 - ▶ The **number of bits** in the ADC output or DAC input word.
 - ▶ The **size** (in Volts, millivolts, microvolts, etc.) of the average analog quantity representing one LSB.

Resolution



Resolution is the

1. **Number of bits** at the ADC output or DAC input.
2. **Size** of the average analog quantity representing one LSB.

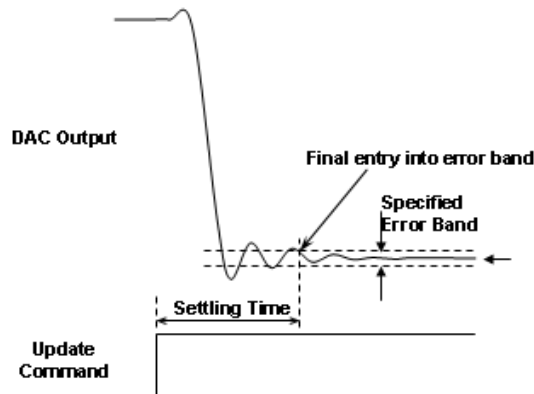
- 3. Both of these are correct
- 4. Neither of these is correct

1 Answer: 3. Both of these are correct

4.

Settling Time

- **Settling Time** of a DAC is the time from a change in the input code until a DAC's output signal enters and remains within the **specified tolerance** of the final value.



Settling Time

Q Settling Time of a DAC is the time from a change in the input code until a DAC's output signal enters and remains within 1/2 LSB of the final value.

- 1. True
- 2. False

1 Answer: 2 - False - - - - By definition, how close the output must be to its final value *must be stated in the specification* and is **not** necessarily 1/2 LSB.

5.

Signal-to-Noise and Distortion (SINAD)

- **Signal-to-Noise And Distortion (SINAD)** is the ratio of the energy (power) in the single-frequency input signal to the power in the remaining energy in the specified bandwidth, including all harmonics, but **not** including d.c.
- Look at the components of SNR, THD and SINAD and you will easily see that SINAD combines SNR and THD.
- SINAD can be calculated by combining SNR and THD in an RSS (root sum squared) manner. The two exponents here should be negative. **THD** is not shown here with a negative sign because it is usually a **negative number**.

$$\text{SINAD} = \sqrt{10^{\frac{-\text{SNR}}{10}} + 10^{\frac{\text{THD}}{10}}}$$

SINAD

Q

SINAD is a combination of

- 1. THD and ENOB
- 2. SNR and THD
- 3. SNR and SFDR

4. None of these is correct

1 Answer: 2 - SNR and THD

6.

Signal-to-Noise Ratio (SNR)

- **Signal-to-Noise Ratio (SNR)** is the ratio of the rms power in the input signal frequency at the output to the rms value of the sum of the power in all other spectral components below one-half the sampling frequency, **not** including **d.c.** or the **harmonics** used to calculate THD.
- Those harmonics that are **not** used to calculate THD **are** included in the SNR calculation.
- **Signal-to-Noise Ratio** is usually expressed in dB.
- In a well-designed data converter, most of the noise is quantization noise.

SNR

Q

Most of the noise in a well designed converter consists of

1. Shot Noise
2. Thermal Noise
3. Quantization Noise
4. None of these is correct

1 Answer: 3 - Quantization Noise

7.

Small Signal Bandwidth

- **Small Signal Bandwidth** is the frequency width over which a circuit will pass these frequencies with a specified limit to the output amplitude variation, assuming the amplitudes of all input frequencies are the same.
- **Small Signal Bandwidth** is specified at some defined amplitude below full scale. This amplitude may differ from product to product.

Small Signal Bandwidth

Q

Small Signal Bandwidth is defined at an amplitude of

1. Full Scale
2. Zero Scale
3. 20 dB below full scale (-20 dBFS)
4. None of these is correct

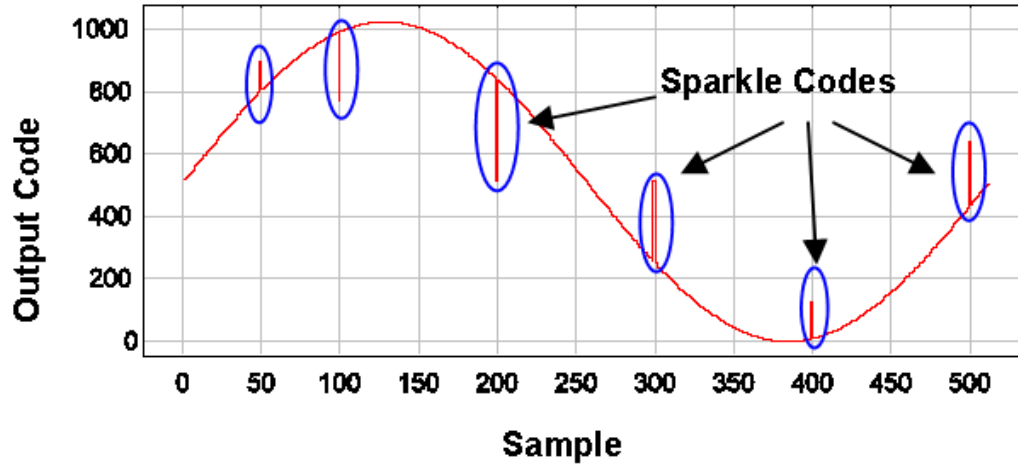
1 Answer: 4 - None of these is correct - - - - It is as defined in the individual data sheet. 20 dB below full scale might be correct in some cases, but is not necessarily correct.

8.

Sparkle Codes

The user is concerned with the effects of metastability on ADC performance, which show up as Bit Error Rate (BER), which is not specified on most ADC data sheets. The error codes that result are often referred to as "sparkle codes", "flyers" or "rabbits". These error codes are large and are often of a binary weighted size.

- **Sparkle codes** in an ADC are large code errors.



- **Sparkle codes** can be prevented by careful design of the ADC.
- **Sparkle code** susceptibility is not generally specified on the data sheet.
- **Sparkle codes** can lead to a high bit error rate (BER)
- "Flyers" or "rabbits" are other names sometimes given to **sparkle codes**.
- **Sparkle codes** are generally binarily weighted in value.

Sparkle Codes

Q

1 Sparkle codes

1. Improve ADC performance
2. Are usually not on data sheets
3. Both of these are correct
4. Both of these is correct

1 Answer: 2 - Are usually not on data sheets

Q

2 Sparkle codes

1. Are large ADC code errors
2. Always go to full scale
3. Both of these are correct
4. Neither of these is correct

2 Answer: 1 - Are large ADC code errors

Q

3 In a code sequence of 141 - 150 - 512 - 156 - 157 . The code that is probably a sparkle code is

1. 150
2. 512
3. 156
4. None of these is correct

3 Answer: 2 - 512 - - - - This code is so far away from the rest of the sequence that it is probably a bad one, or a sparkle code.

9.

Spectral Leakage

- **Spectral Leakage** is the "leaking" of energy from one frequency line on the Frequency domain plot (FFT Plot) to other frequency "lines".
- **Spectral Leakage** causes a reduction of **Spectral Resolution** because it spreads or "leaks" some energy from the proper "line" or "bin" of the Frequency Domain plot into adjacent "lines" or "bins".

Spectral Leakage



Spectral Leakage occurs when energy from one spectral bin "leaks" into adjacent bins.

1. True
2. False

1 Answer: 1 - True

10.

Spectral Resolution

- A frequency "line" or bin is one of the many vertical bars that make up the frequency domain plot.
- In a frequency domain (FFT) plot, **Spectral Resolution** is a measure of how small a range of frequencies is represented by each frequency "line" of bin.
- That is, it indicates how well frequency is "resolved" in the plot.
- **Spectral Resolution** has **nothing** to do with bits.

Spectral Resolution



Spectral Resolution is the number of bits used to create the frequency domain plot.

1. True
2. False

1 Answer: 2 - False

11.

Spurious Free Dynamic Range (SFDR)

- **Spurious Free Dynamic Range** (SFDR) is the difference between the level of the desired output signal and the value of the highest amplitude output frequency that is not present in the input.
- **Spurious Free Dynamic Range** should NOT be confused with **Input Dynamic Range**.
- **Spurious Free Dynamic Range** is usually expressed in dB and measured in the frequency domain.

Spurious Free Dynamic Range



Spurious Free Dynamic Range and **Input Dynamic Range** are different names for the same thing.

1. True
2. False

1 Answer: 2 - False

12.

Static Specifications

- **Static Specifications** are those specifications of a data converter pertaining to static (d.c.) or very slowly moving conditions.
- **Static Specifications** include *gain error*, *offset error*, *differential* and *integral linearity errors* and *Total Unadjusted Error*.

Static Specifications



Static Specifications include

1. Gain and Offset errors
2. Differential and Integral Linearity errors
3. Total Unadjusted Error
4. All of these

1 Answer: 4 - All of these

T - Z

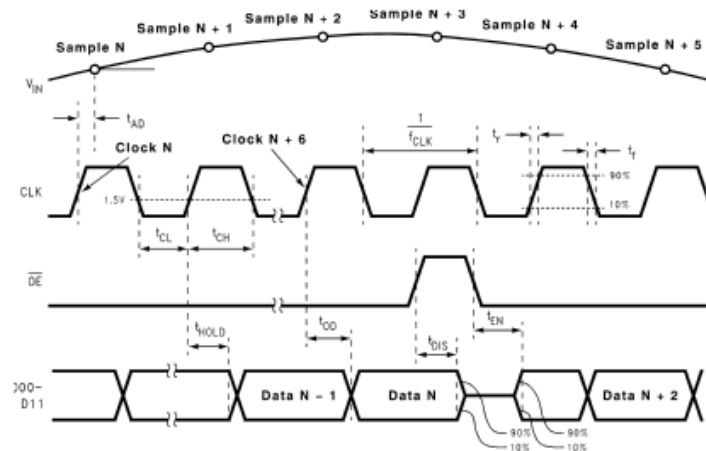
Terms beginning with letters "T" through "Z".

- 9.1 Throughput Rate
- 9.2 Throughput Time
- 9.3 Time Domain Plot
- 9.4 Total Harmonic Distortion (THD)
- 9.5 Total Unadjusted Error
- 9.6 Update Rate

1.

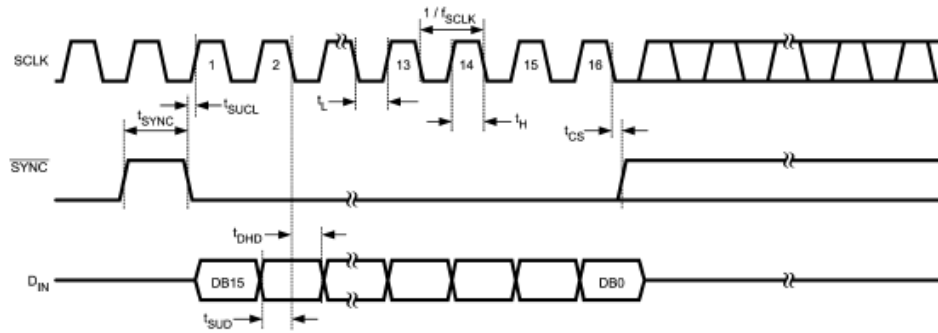
Throughput Rate

- Throughput Rate is the maximum continuous conversion rate of the ADC or DAC.
- Another way of saying this is the **Sample Rate** of an ADC or the **Update Rate** of a DAC.
- ADC **Sample Rate** and DAC **Update Rate** should not be confused with **Clock Rate**.
 - ▶ For High Speed ADCs and DACs with a parallel data bus, ADC **Sample Rate** and DAC **Update Rate** are usually the same as the **Clock Rate**. An example is shown in the ADC12D040 Timing Diagram here, where there is one conversion for each clock cycle.

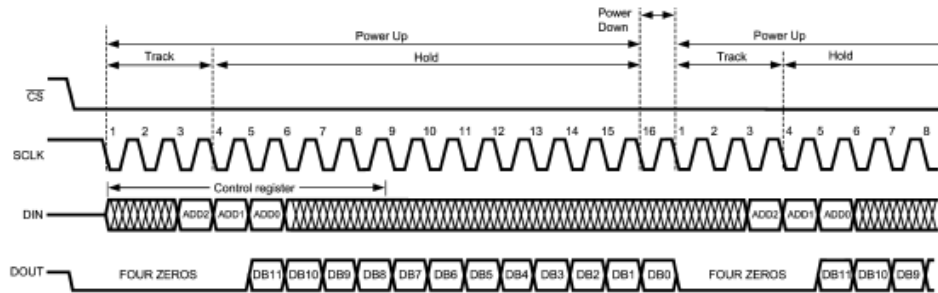


- ▶ For General Purpose ADCs, with a parallel data bus, the ADC Sample Rate **may or may not** be the same as the ADC **Clock Rate**, whereas general purpose ADCs with a serial data bus will have a clock rate that is a multiple of the sample rate.
- ▶ The DAC update rate for General Purpose DACs with a parallel data bus is *usually*, but not always, the same as the DAC clock rate.
- ▶ The DAC update rate for General Purpose DACs with a serial data bus is **not** the same as the DAC clock rate. The clock rate

will be **higher** than the sample rate, as indicated with the DAC121S101 Timing here.



- ▶ For General Purpose ADCs and DACs with a serial data bus, the clock rate is usually a multiple of the ADC conversion rate or the DAC update rate. An example is shown in the ADC128S102 Timing Diagram here, where 16 clock cycles are required for a single conversion.



Throughput Rate

Q

1 Throughput rate of an ADC is the same as

1. Clock frequency
2. Sample rate
3. Both of these are correct
4. Neither of these is correct

1 Answer: 2 - Sample rate

Q

2 Clock rate and sample rate

1. Are always the same
2. Can be the same in some ADCs
3. Are never the same

2 Answer: 2 - Can be the same in some ADCs

2.

Throughput Time

- **Throughput Time** is the time it takes a converter to acquire a signal, convert it and output the data.
- **Throughput Time** should not be confused with **Conversion Time**, which is a component of **Throughput Time**.

Throughput Time

Q

Throughput Time and **Conversion Time** are the same

1. True

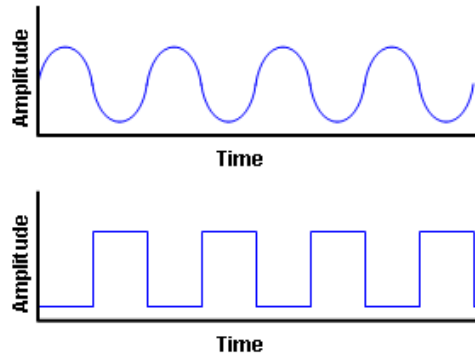
2. False

1 Answer: 2 - False

3.

Time Domain Plot

- A **Time Domain Plot** is a plot of signal amplitude or level vs. time.
- A **Time Domain Plot** is what we normally think of when we consider a waveform.
- Examples of time domain plots are shown here



Time Domain Plot

Q

A Time Domain Plot is

1. What we normally think of when thinking of a waveform.
2. A plot of amplitude or level vs. time
3. Both of these are correct
4. Neither of these is correct

1 Answer: 3 - Both of these are correct

4.

Total Harmonic Distortion (THD)

- **Total Harmonic Distortion (THD)** is the ratio, expressed in dB or dBc, of the rms total of the first specified number of harmonic components at the output to the rms level of the input signal frequency as seen at the output.
- **Total Harmonic Distortion** is calculated as indicated here, where A_{r1} is the RMS power of the input frequency at the output and A_{r2} through A_{rn} are the RMS power in the first "n" harmonic frequencies.

$$\text{THD} = 20 \times \text{Log}_{10} \sqrt{\frac{A_{r2}^2 + \dots + A_{rn}^2}{A_{r1}^2}}$$

- Specifying fewer harmonics for **THD** can provide a better **THD** figure.
- Specifying more harmonics for **THD** can make **THD** look worse than it actually is.
- The number of harmonics specified for **THD** has no effect upon SINAD and ENOB.

THD



Specifying fewer harmonics for THD

1. Can sometimes make the THD figure look better than it really is
2. Can sometimes make the THD figure look worse than it really is
3. Can sometimes make the SINAD figure look better than it really is
4. Can sometimes make the SINAD figure look worse than it really is

1 Answer: 1 - Can sometimes make the THD figure look better than it really is



Total Unadjusted Error

- **Total Unadjusted Error (TUE)** is the worst deviation found from the ideal transfer function.
- **Total Unadjusted Error** is a comprehensive specification which includes full scale error, linearity error, and offset error.
- **Total Unadjusted Error** is a useful specification only when it can be specified as no worse than 1 or 2 LSB. As such, it is seldom found on data sheets of converters with greater than 8 bit resolution.

Total Unadjusted Error



1 **Total Unadjusted Error** is a specification that includes

1. Offset, Gain and Linearity Errors
2. SNR and THD
3. Both of these are correct
4. Neither of these is correct

1 Answer: 1 - Offset, Gain and Linearity Errors



2 **Total Unadjusted Error** is

1. Found on all converter data sheets
2. A common specification for 12-bit ADCs
3. Both of these are correct
4. Neither of these is correct

2 Answer: 4 - Neither of these is correct - - - - Generally found only on some 8-bit ADC data sheets



Update Rate

- **Update Rate** of a DAC is the speed at which the output is changed or updated. That is, **Update Rate** is the rate at which the DAC output can be updated.
- Do not confuse **Update Rate** with **Clock Rate** or **Clock Frequency**.

Update Rate



1 Update Rate

1. is a DAC specification.
2. Indicates how quickly the DAC output can be updated.
3. Both of these are correct.

4. Neither of these is correct.

1 Answer: 3 - Both of these are correct.



2 Update Rate is the same as clock rate or frequency.

1. True

2. False

2 Answer: 2 - False

IMD

See Intermodulation Distortion

ADC

Analog-to-Digital Converter

BER

See Bit Error Rate

Conversion Latency

See Pipeline Delay

DAC

Digital-to-Analog Converter

DLE

Differential Linearity Error

DNL

Differential Non-Linearity

Effective Bits

See Effective Number of Bits (ENOB)

ENOB

Effective Number of Bits

FFT

See Fast Fourier Transform. Also, a frequency domain plot is sometimes referred to as an FFT.

ILE

Integral Linearity Error

INL

Integral Non-Linearity

Latency

See Pipeline Delay

LSB

Least Significant Bit

MSB

See Most Significant Bit

Output Glitch

See Glitch

PSRR

See Power Supply Rejection Ratio

S/(N+D)

See SINAD

Sampling Delay

See Aperture Delay

SFDR

See Spurious Free Dynamic Range.

SINAD

Signal to Noise and Distortion Ratio

SNDR

See SINAD.

SNR

See Signal-to-Noise Ratio

SSBW

See Small Signal Bandwidth

THD

See Total Harmonic Distortion

TUE

See Total Unadjusted Error

V_{REF}

The converter reference voltage.

Zero Error

See Offset Error

Zero Scale Error

See Offset Error

Zero Scale Offser Error

See Offset Error

Zero Scaqlle Offser Error

Frequently Asked Questions

Do you have a question? We may have already answered it. Check below to see if you can find the answer to your question.

Questions

Answers

● **Contact/Help Information**

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Thank you,
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